
# Rigger Micro Technologies

Total solution of advanced IC packaging

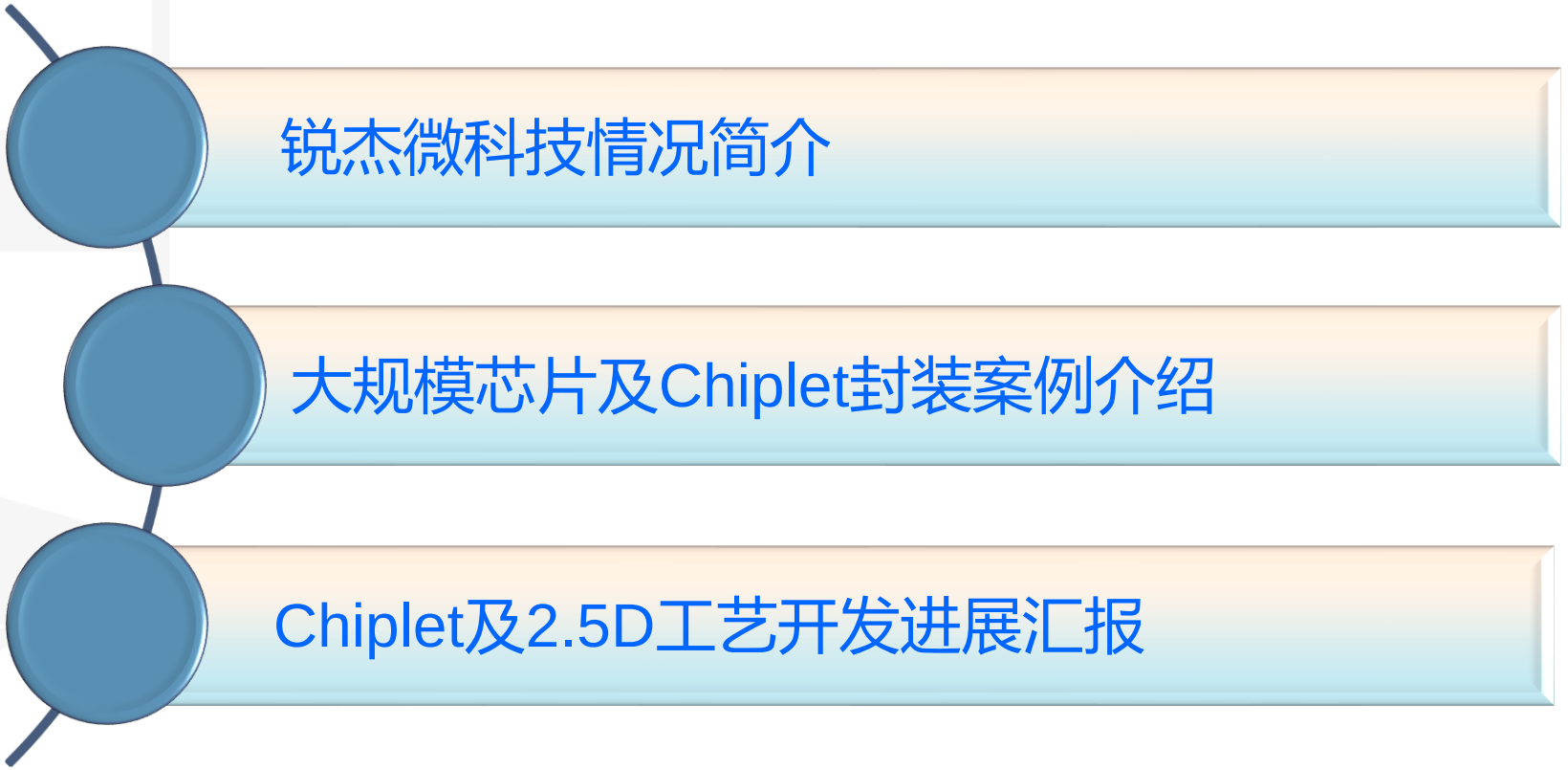
Rigger Micro Technologies

# 锐杰微科技高端芯片及chiplet封装案例分享

方家恩

2023.12.08

# 内容



# 集团概况

| | |
|---|---|
| 愿景 | 成为全球领先的集成电路高端封测方案服务商 |
| 使命 | 帮助国内高端核心芯片完成国产化封测 |
| 价值观 | 品质为本，攻坚克难，勇于创新 |

锐杰微科技（简称RMT）是一家**提供全流程Chiplet&高端芯片封测方案商**。聚焦高端芯片封装设计&仿真、规模化加工制造及成品测试；**具有数百项芯片封装项目管理和交付经验**，已服务超过200家科研院所及高端商业客户。

RMT拥有行业领先的封装设计&仿真、制造和成品测试团队。已建立一套完整的封装设计标准、生产管控流程、质量保证体系；**配备先进规模化的封测产线。**

RMT致力推动国内产业合作，作为中国Chiplet标准的发起方，**参与行业标准制定**并提供国产化专用芯片研发配套及封装工艺平台。

未来，RMT将在研发和产能层面不断投入，秉承“**品质为本，攻坚克难，勇于创新**”的理念，以“**帮助国内高端核心芯片完成国产化封测**”为使命，致力于为客户提供卓越的产品和服务。


# 集团布局

**郑州封测基地**
- 综合类封测制造基地
- 2条FcBGA，fcCSP, WB等
- 车规封测基地
- Bumping、TSV、硅载板加工基地


**办事处**






**市场&销售中心**




**成都研发，销售办事处**


**办事处**




**集团总部&苏州封测基地**
- 先进封装研究院
- 研发中心
- 工程技术中心

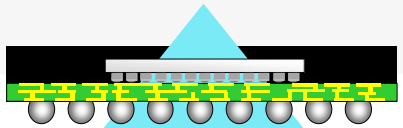
**苏州封测基地**
- 8条FCBGA
- 4条Chiplet（2D+2.5D）
- CP/FT/SLT

# 产品能力-2D及2.5D工艺全流程

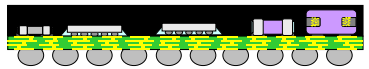
Now

2023

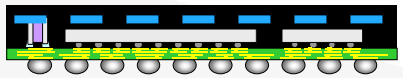
## 传统+高阶封装



FCCSP



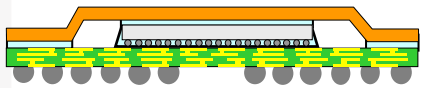
SiP



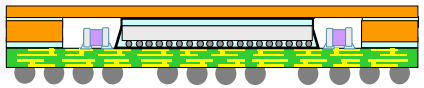
MCM (FC die) molded package

Molded hybrid package

WB BGA (CSP)



FCBGA with HS



FCBGA with Stiffener

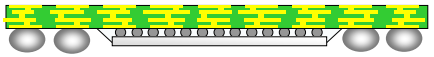
QFN

SOP

## 高阶、复杂工艺封装

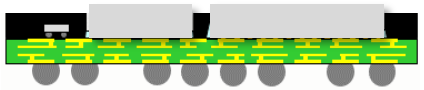
Dual side FC

SSD FCCSP

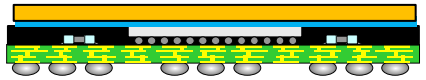


FC with AiP

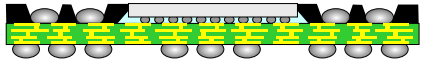
## 高效散热封装



MCM exposed die (FAM)

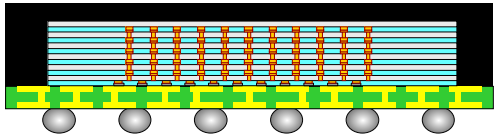


Exposed die (FAM) + H/S

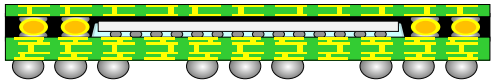


Exposed die (FAM) MLP-PoP

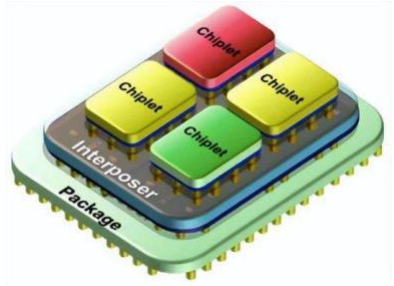
## TSV+2.5D/3D封装



SSD FCCSP (TSV)



Laminate interposer-PoP




Chiplet

# ➢Chiplet 设计开发工具----2D及2.5D设计仿真全流程

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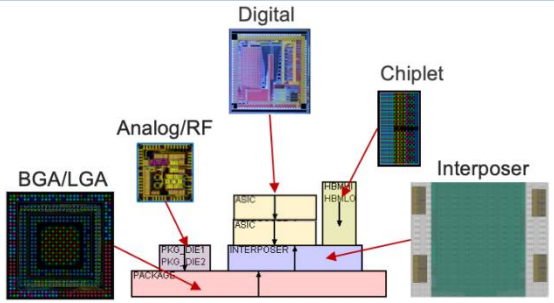
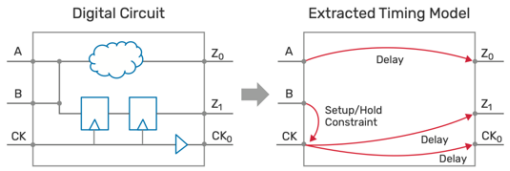
## Top-Level Planning, P&R and Sign-Off

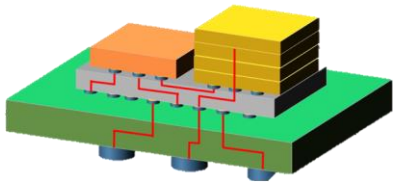
### Integrity



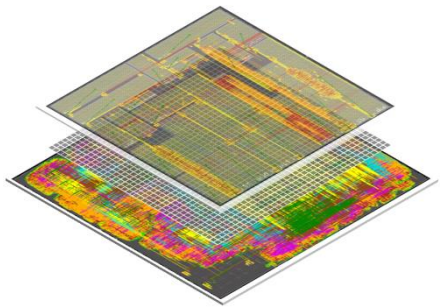

Top-Level Aggregation and Optimization



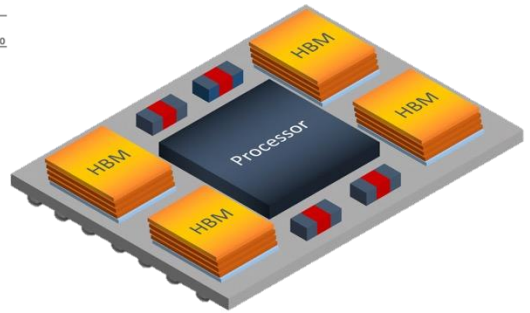

STA



Sign-Off DRC/LVS



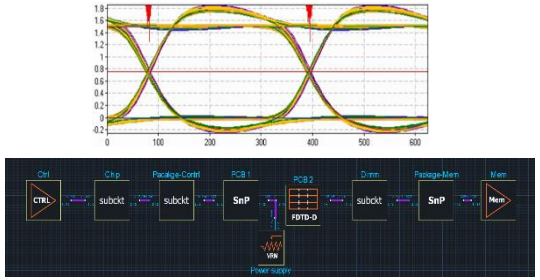
2.5D/3D Integration Place & Route



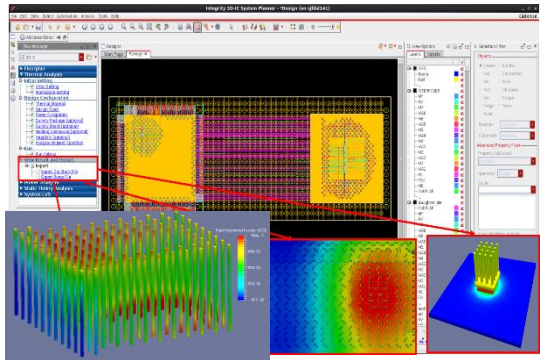

Silicon (TSV) interposer

## System-Level Analysis

### Celsius, Clarity & Sigrity



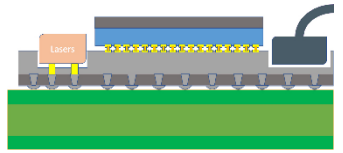
Pre- & Post-Route Signal Integrity
Chiplet-to-Chiplet Electrical Compliance



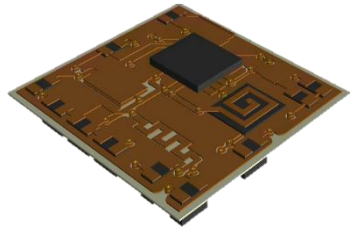
Early-Stage Through Sign-off
Thermal/Power Analysis

## Analog/RF

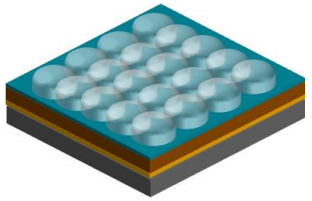
### Virtuoso




Co-Packaged Optics



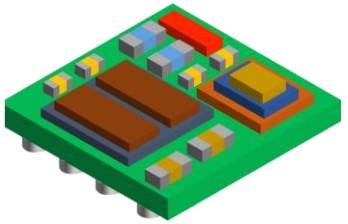
RF Module



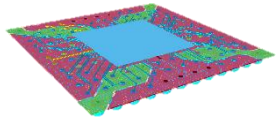
CIS

## Packaging

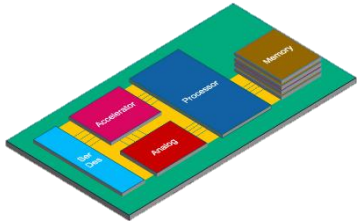
### Allegro



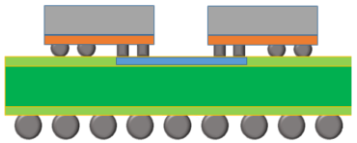
Laminate SiP/MCM



FOWLP




RDL Interposer



Interconnect Bridge

Mixed-Technology, Multi-Domain Common Hierarchical Database

# 业务范围

RMT Rigger Micro Technologies

## 高端芯片先进封测一站式解决方案
## —提升产品集成度与性能指标，降低产品功耗

### 封装设计&仿真

- ✓ 评估/制定芯片封装方案
- ✓ 芯片Floor plan设计建议
- ✓ Bump/ball map设计
- ✓ 封装基板设计与仿真

### 封装加工制造

- ✓ RDL&Bumping加工
- ✓ CP测试
- ✓ 工程批
- ✓ 小批量
- ✓ 量产

### 成品测试

- ✓ FT/SLT测试
- ✓ 测试夹具及物料采购
- ✓ 探针卡/测试板/产品板/老化板开发
- ✓ 委托芯片考核与鉴定

### 先进材料采购服务

- ✓ 提供专业配套晶圆和先进材料的采购服务

### 流片服务

- ✓ 提供MPW服务
- ✓ 提供Full Mask服务

### 板级电路开发服务

- ✓ 系统级电路开发
- ✓ 原理图+PCB设计
- ✓ 板级+系统级仿真
- ✓ PCBA

## 项目服务流程

**需求导入**
（规格、成本、交期）

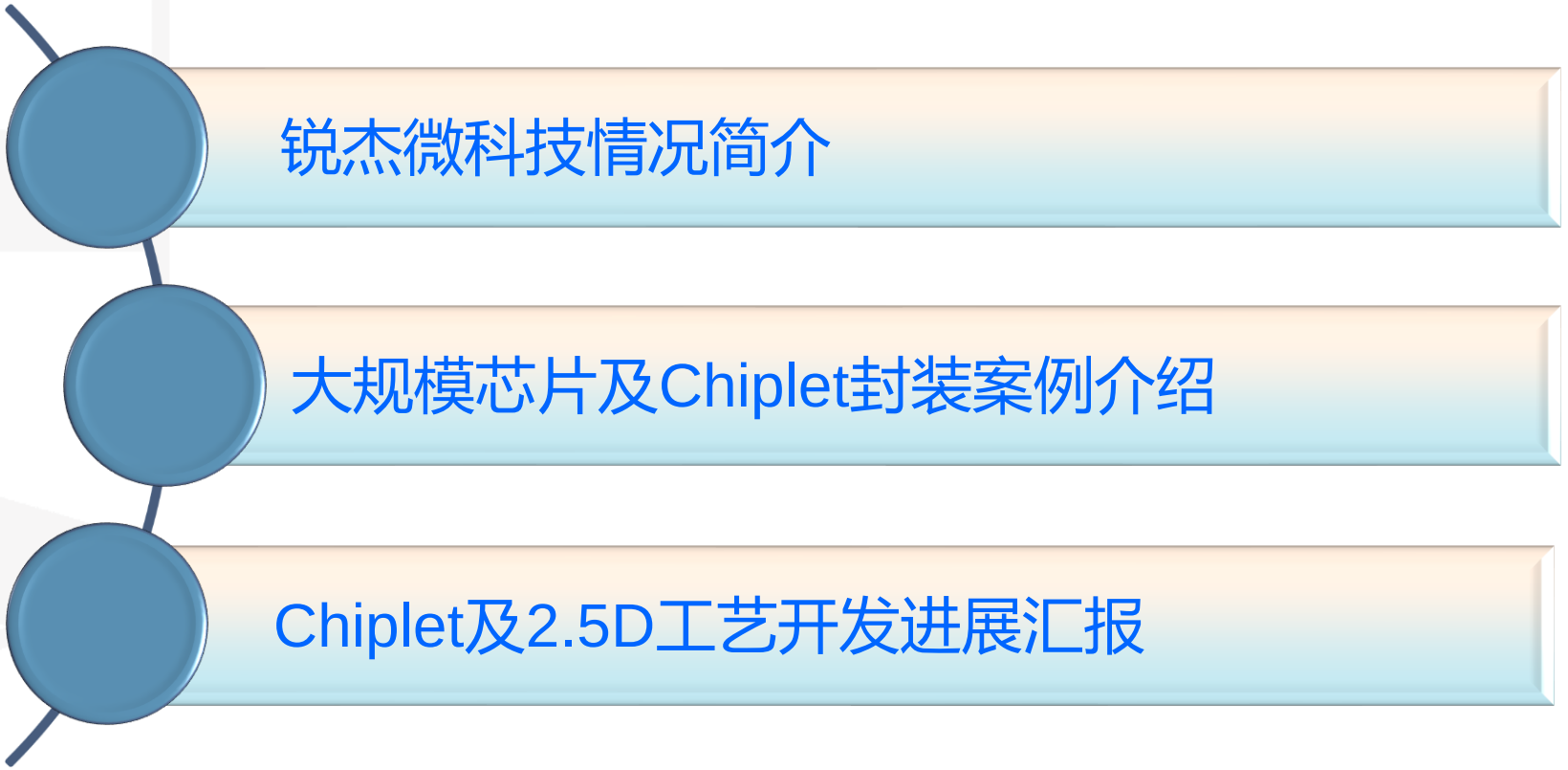
**封装设计&仿真**
（规划、结构、材料、基板）
（电、热、机械、联合仿真）

**封装加工制造**
RDL&Bumping、CP测试）
（工程批/小批量/量产）

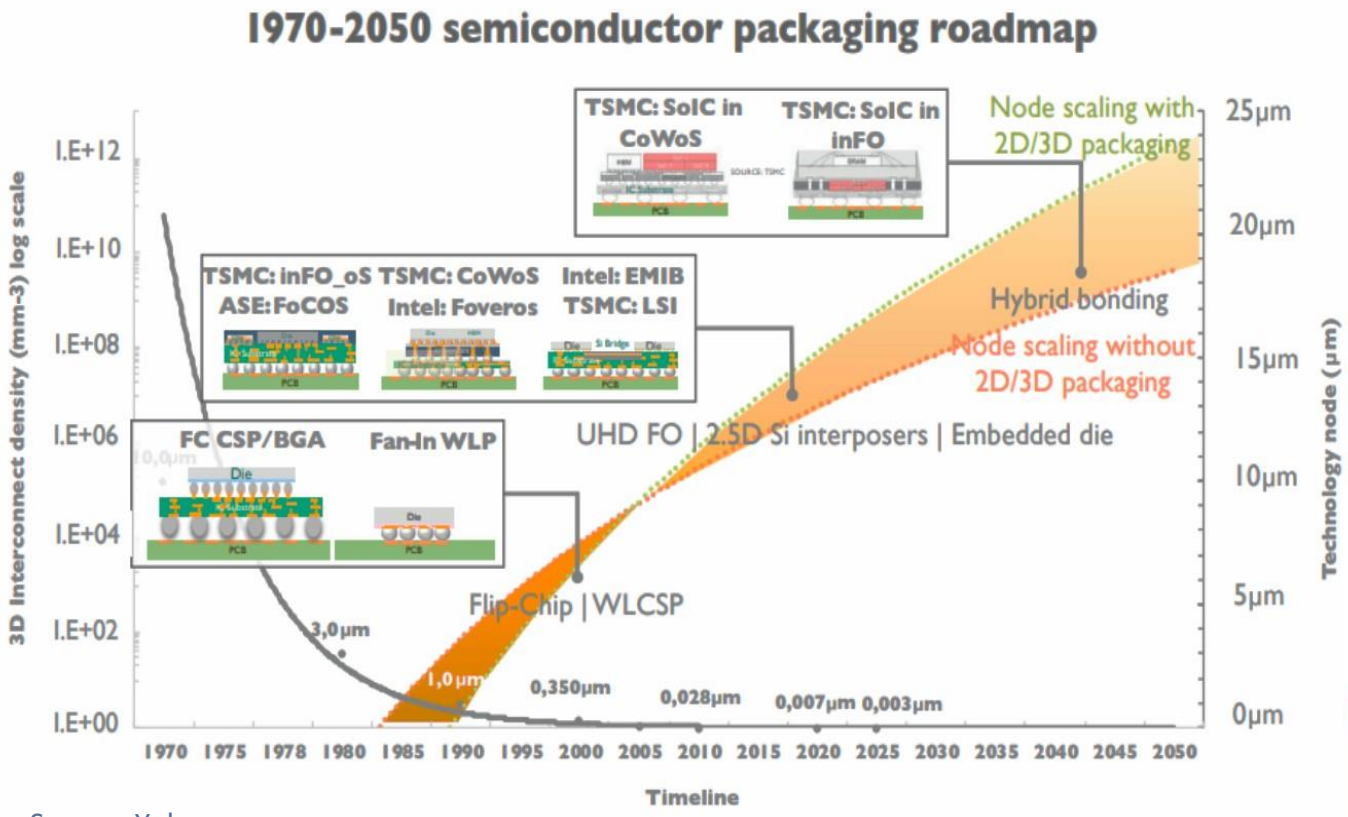
**成品测试**
（FT/SLT测试）

**项目验收**
（设计报告、仿真报告、工艺文件）

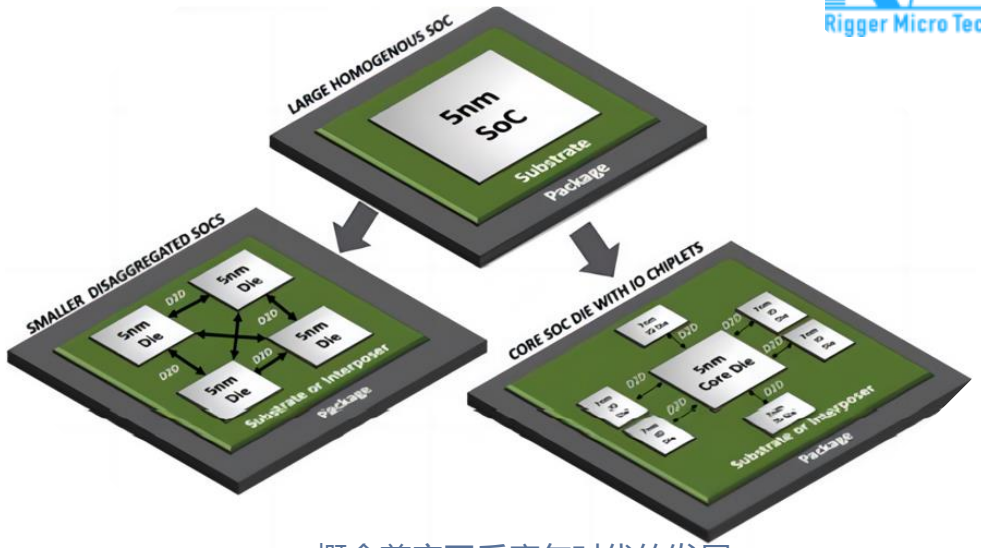
# 内容



# More than Moore
# -半导体封装技术演进路线图

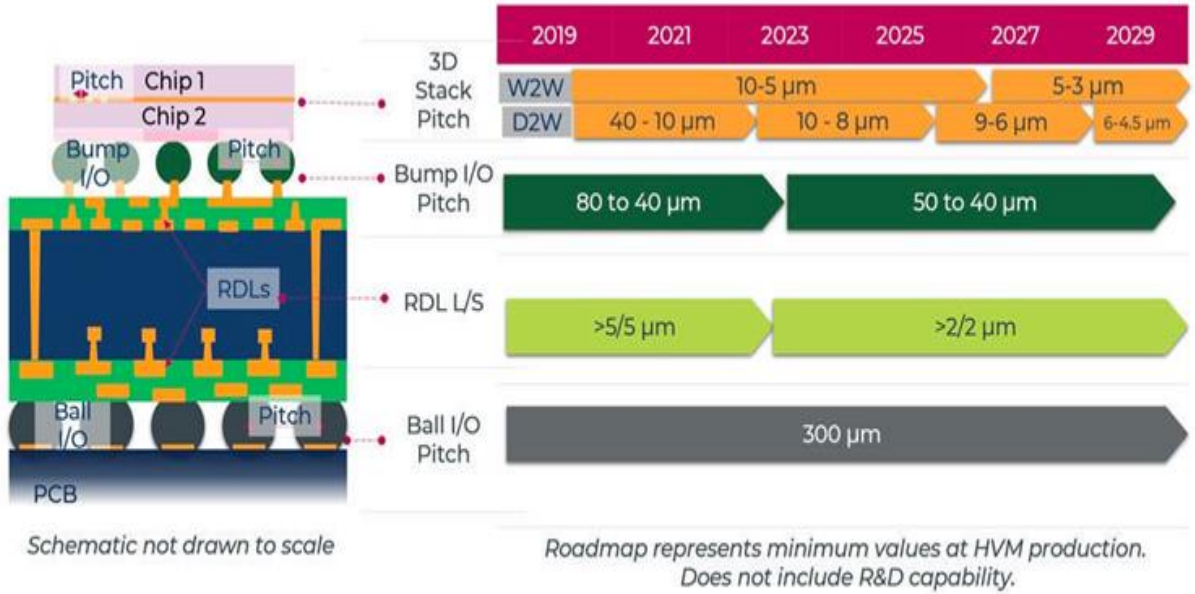



Source: Yole




Chiplet概念奠定了后摩尔时代的发展

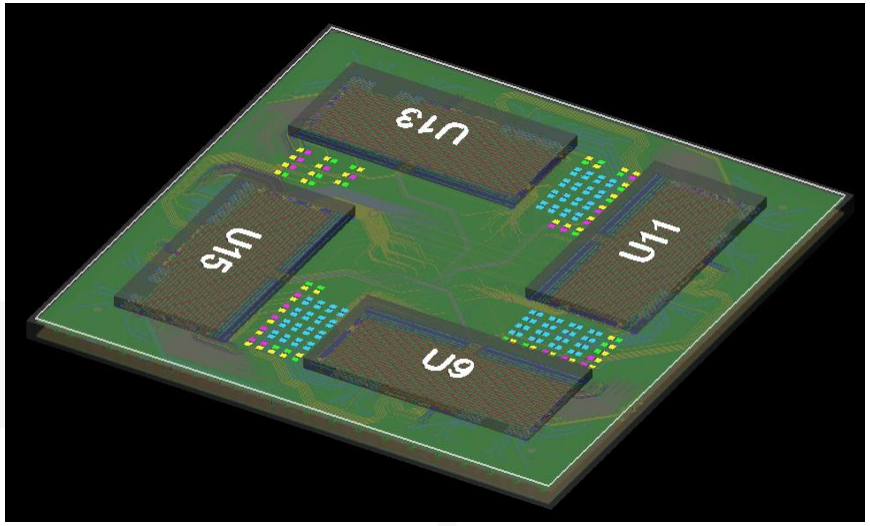
Advanced Packaging Roadmap -IO pitch & RDL L/S




Bump I/O pitch is scaling much faster than Ball I/O pitch which drives a finer RDL L/S at IC substrate package level.

# Chiplet DSP项目概况

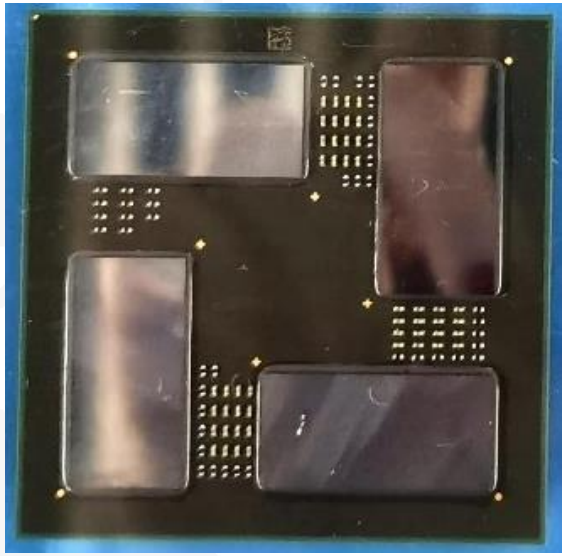
DSP*4



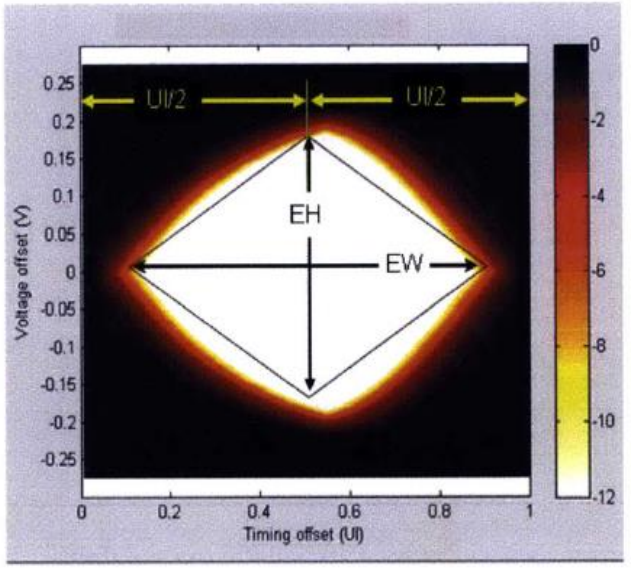

1.204B x4*4  20Gbps

2.SRIO x4*4 20Gbps

3.Power Dissipation:30W Total



| PKG Type | | FCBGA |
|---|---|---|
| PKG Size (mm) | | 40x40 |
| Die Size (mm) | | 17*8.5  x4 |
| Die THK (um) | | 780 |
| Substrate | Layer / THK (mm) | 10L / 1.26 |
| | Core THK (um) | 820 |
| | PP THK (um) | 30 |
| | SR THK(um) | 20 |
| | Core Type | MCL-E705G |
| | PP Type | GZ41 |
| | SR Type | AUS703 |




| | |
|---|---|
| Eye Width (ps) after CTLE | = ~0.3 UI = 37.5 |
| Eye Height (mV) after CTLE | = ~10 |

# 技术特点

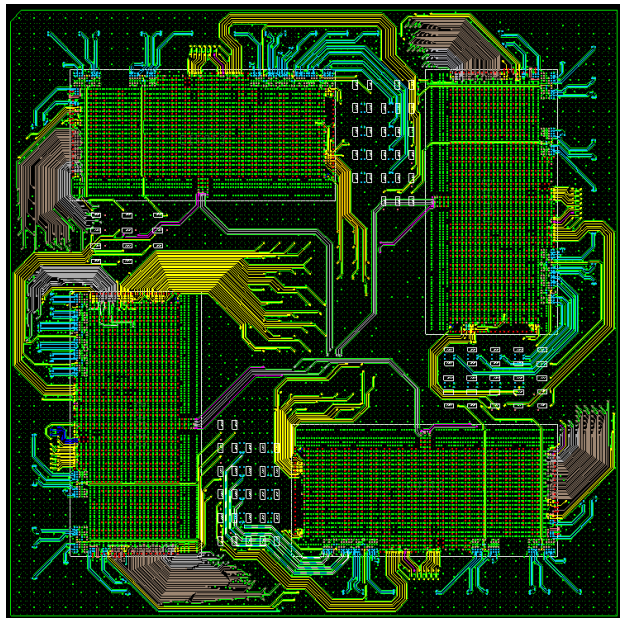
1.多DIE产品的设计：Minimize PKG Size/stackup；

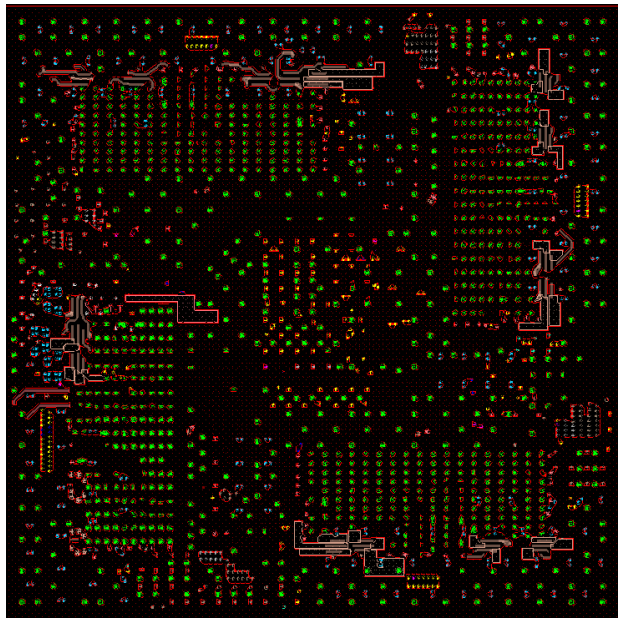
2.多通道互连设计，保证通道间的隔离以及每个通道的信号质量。

a).L2/L4/L7为主要信号走线层，其中主要是芯片之间的互连线以及需要引出的高速信号线以及差分信号线。

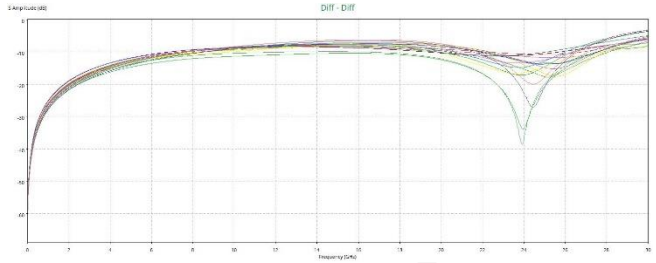
b).L1/L3/L5/L8为地层，在信号层的相邻层设置大面积地平面层，保证信号的电流回路、阻抗完整等指标。

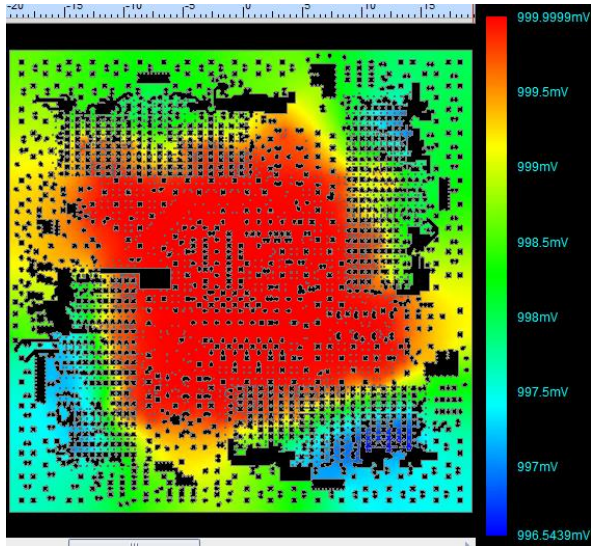
c).L6/L9为主要电源层，大面积的电源平面可以保证电源的回路电感，电源压降、通流量等指标满足要求

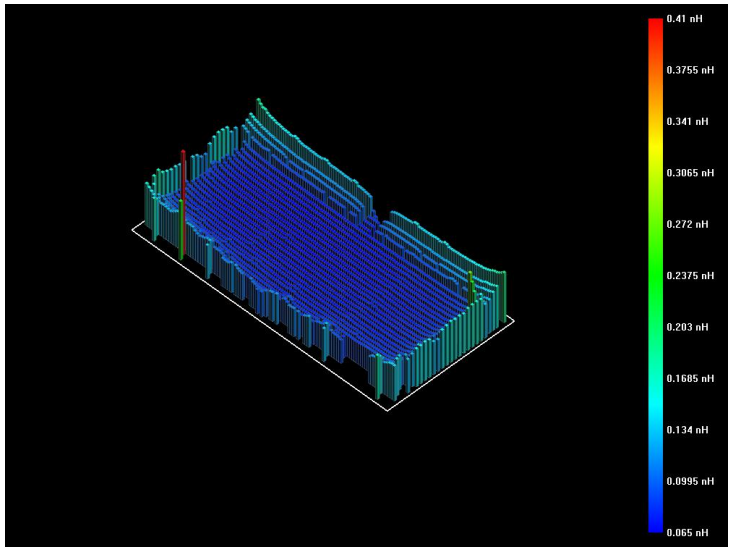


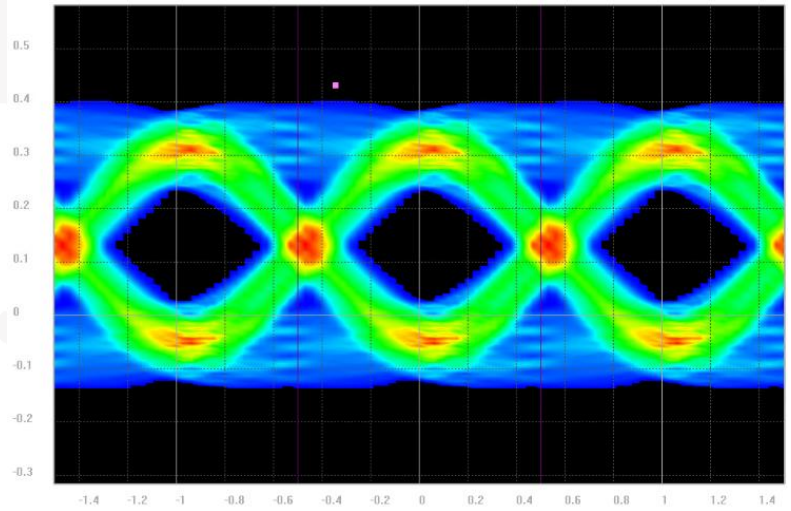


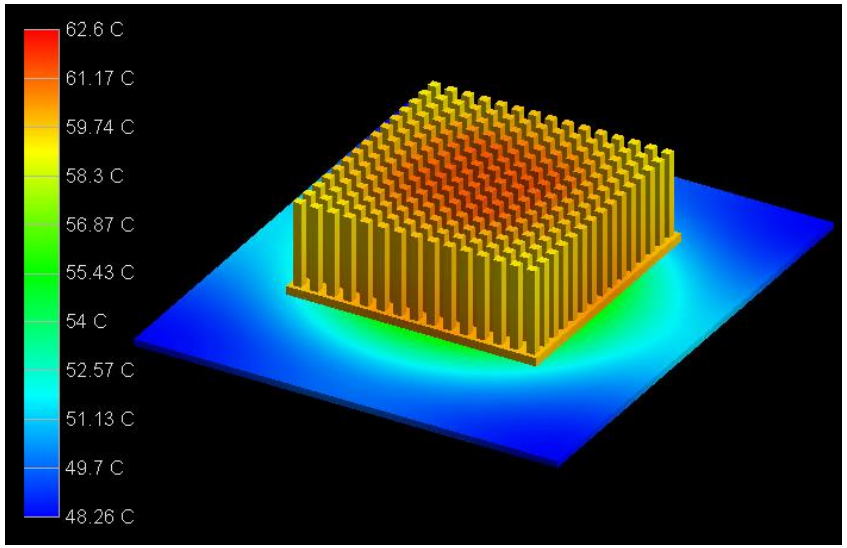
# 部分仿真结果



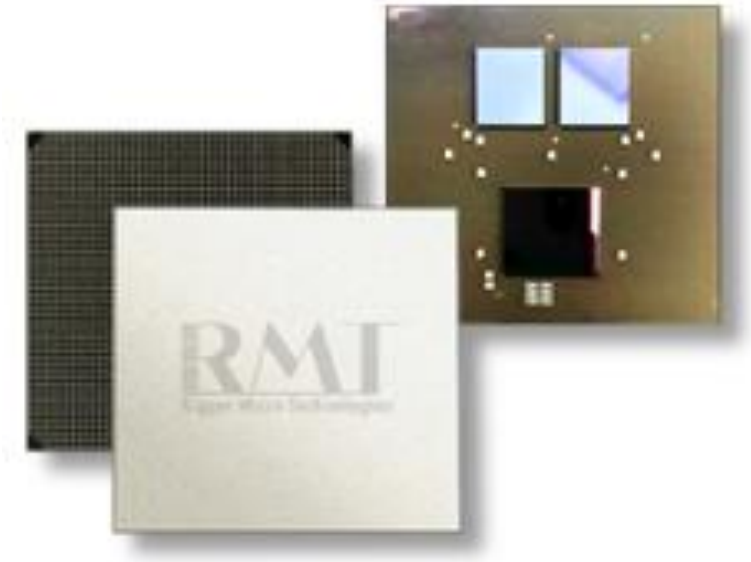



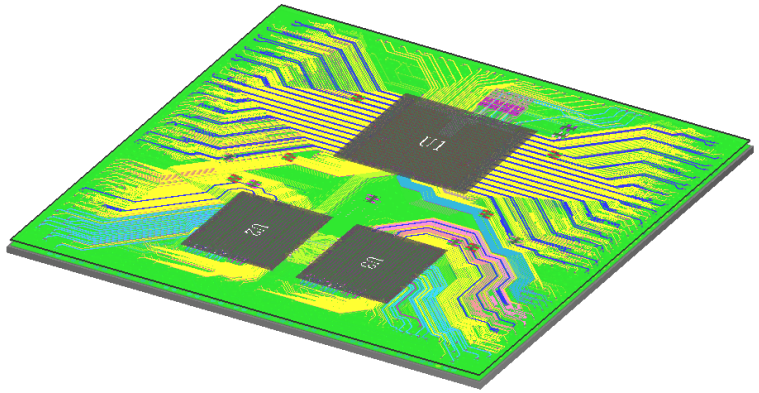



# 双CPU+FPGA



应用领域：Server CPU

| PKG Type | | FCBGA |
|---|---|---|
| PKG Size (mm) | | 61x61 |
| Die Size (mm) | | 16x16;13x11*2 |
| Die THK (um) | | 780 |
| Substrate | Layer / THK (mm) | 10L / 1.25 |
| | Core THK (um) | 820 |
| | PP THK (um) | 30 |
| | SR THK(um) | 25 |
| | Core Type | MCL-E705G |
| | PP Type | GZ41 |
| | SR Type | AUS703 |

主要参数：

1.PCIE 3.0 8Gbps

2.DDR3 1066 Mbps

3.XAUI 6.25Gbps

4.VDD CORE:0.9V 40A

4.Power Dissipation: 50W

Spec：

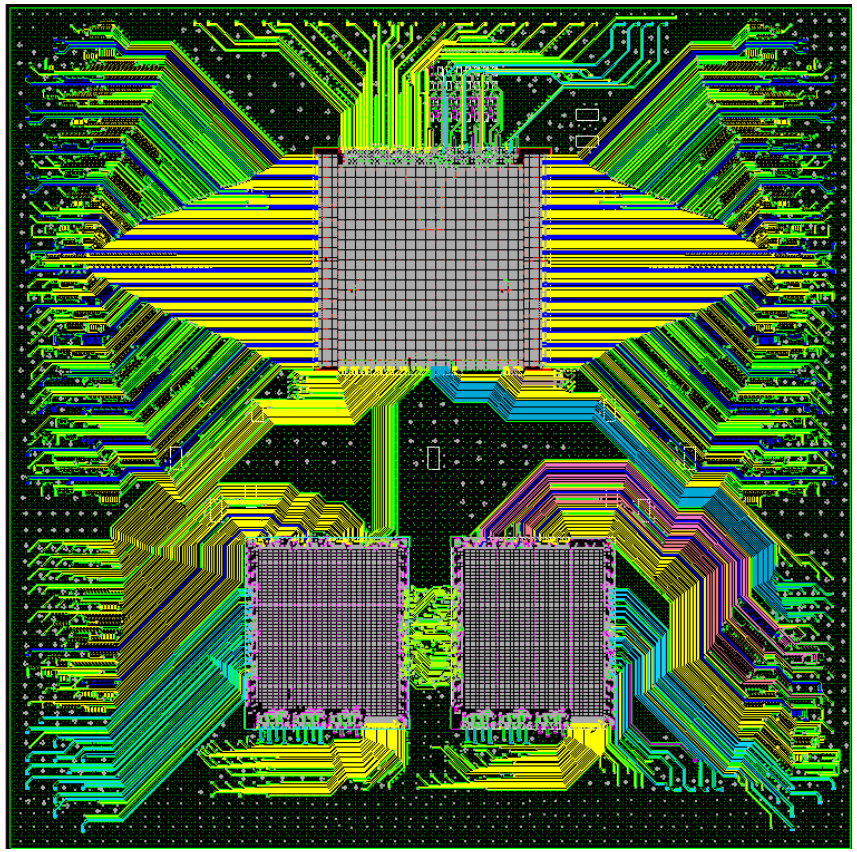
- FPGA：单端 50+/-10%Ω
- 高速信号差分对的阻抗按100+/-10%欧姆管控
- 差损大于-1dB;回损小于-20dB
- 高速差分对N与P的线长要等长，建议按差值≤50um管控；同一个Group内的TX或RX所有差分对线长差异（即Max线长与Min线长的差值），建议按差值≤500um管控。

# 基板设计

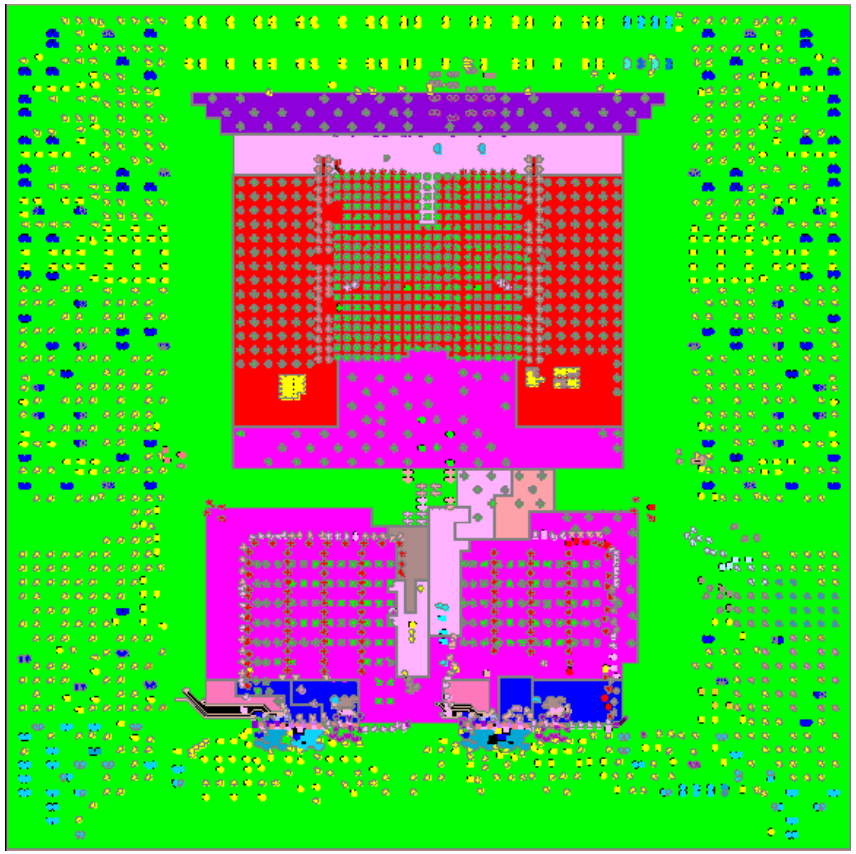
1.高密度走线设计：保证信号质量(两层走线)

a)DQ [0-3] (32+72)*4=416

2.大电流、多电源设计处理

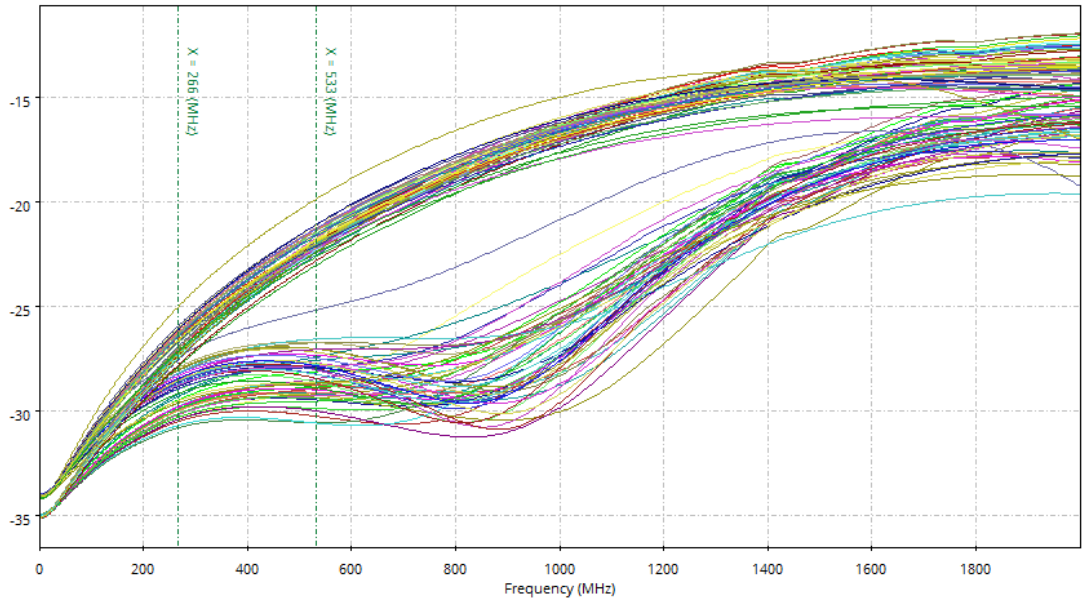


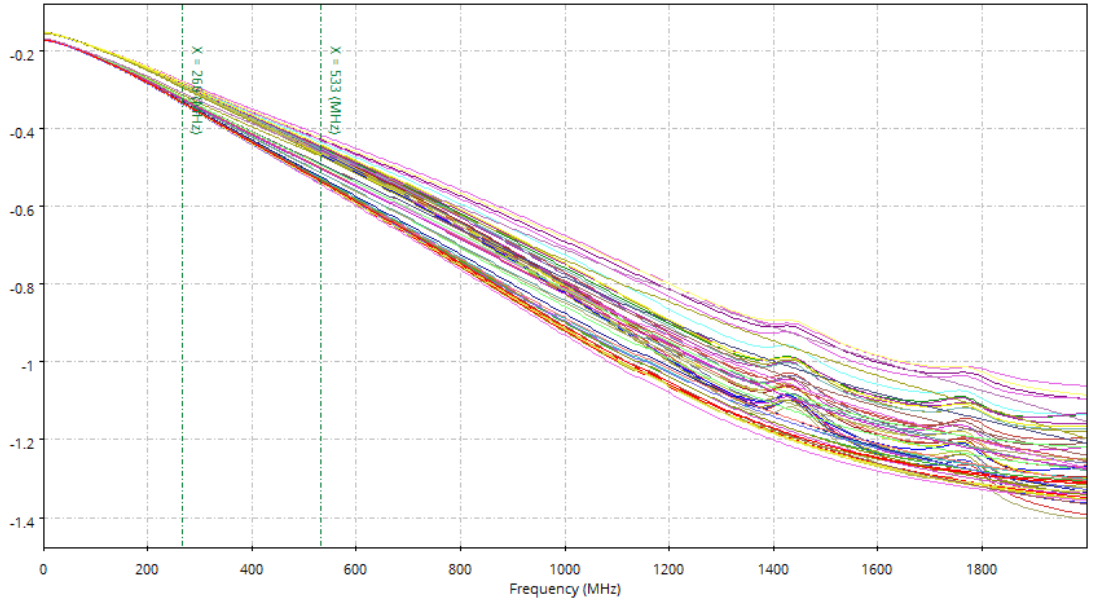
L2

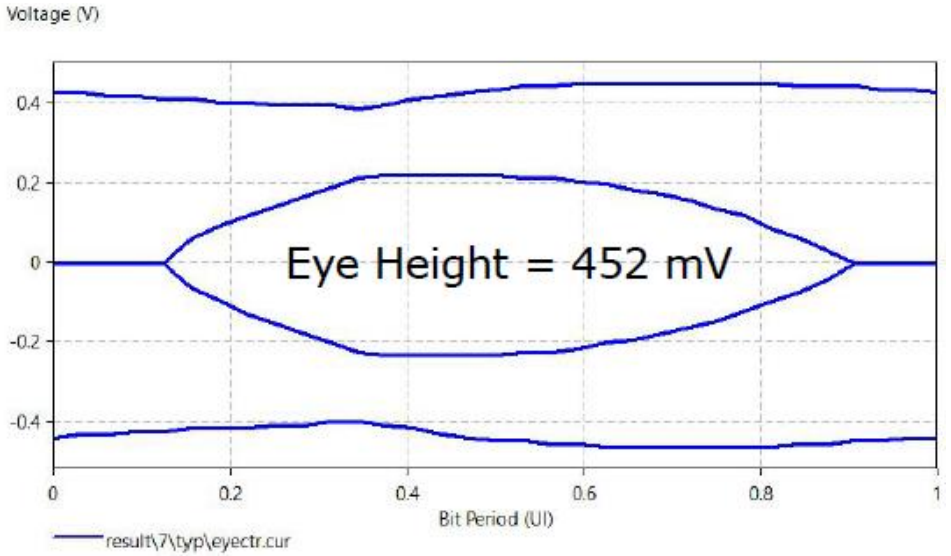


L6

# 部分仿真结果

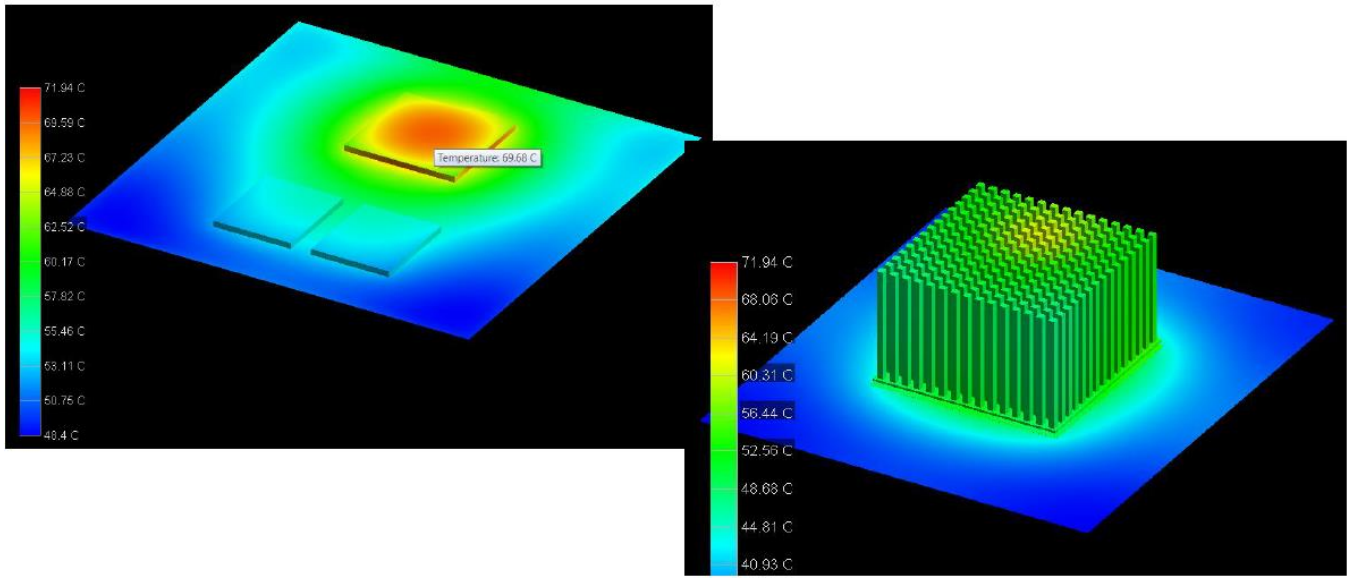


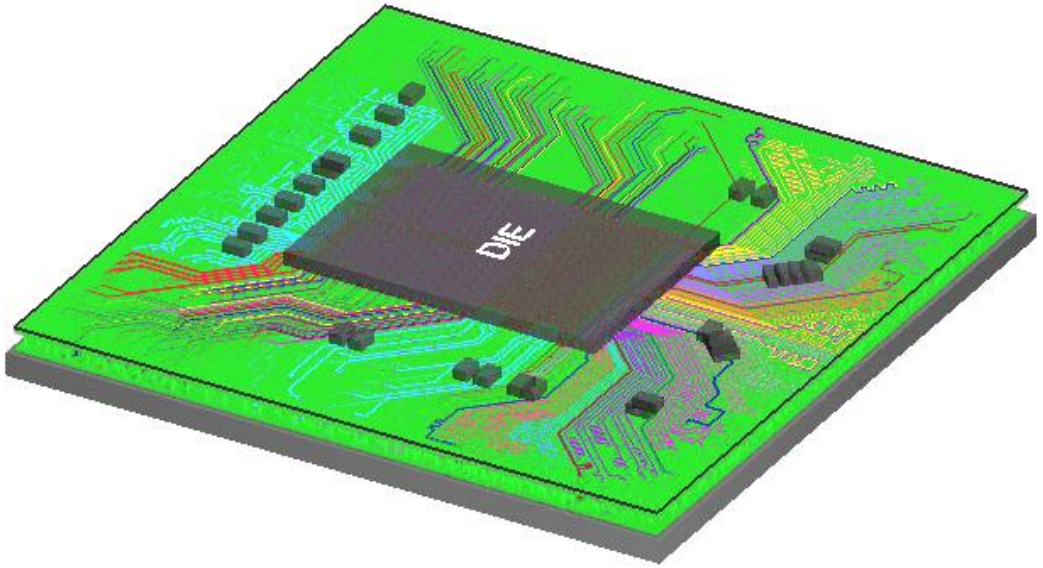




环境温度 25 ℃
环境空气流动速度：3 m/s
加上**铜制散热器**，CPU最高温度为72度左右

| | |
|---|---|
| CPU power (U1) | 40W |
| FPGA power (U2) | 5W |
| FPGA power (U3) | 5W |



# GDDR6产品




应用领域：GPU

| PKG Type | | FCBGA |
|---|---|---|
| PKG Size (mm) | | 37.5x37.5 |
| Die Size (mm) | | 12.5x17.8 |
| Die THK (um) | | 780 |
| Substrate | Layer / THK (mm) | 12L / 1.36 |
| | Core THK (um) | 820 |
| | PP THK (um) | 30 |
| | SR THK(um) | 25 |
| | Core Type | MCL-E705G |
| | PP Type | GL102 |
| | SR Type | AUS703 |

# 主要参数指标

1. GDDR6:16Gbps

2. PCIe 4.0:16Gbps

2. HDMI:6Gbps

3.VDD CORE:0.9V 80A/30A

4. Power Dissipation: 100W

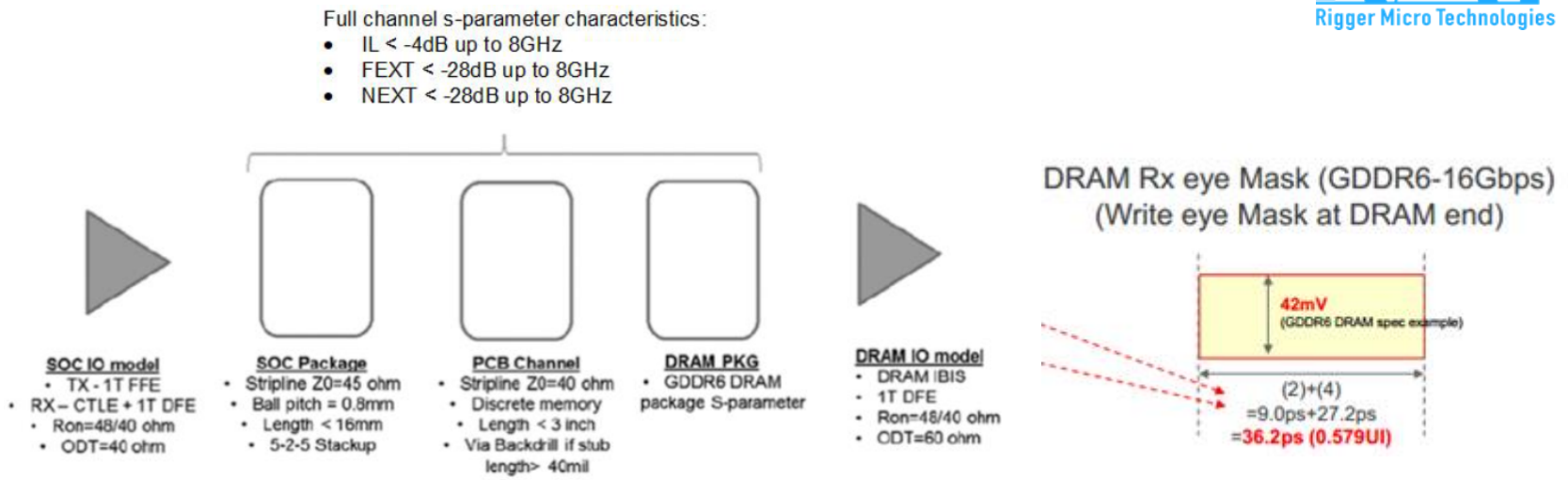



**Figure 4: Typical GDDR6 Reference Channel meeting 16Gb/s Requirements**

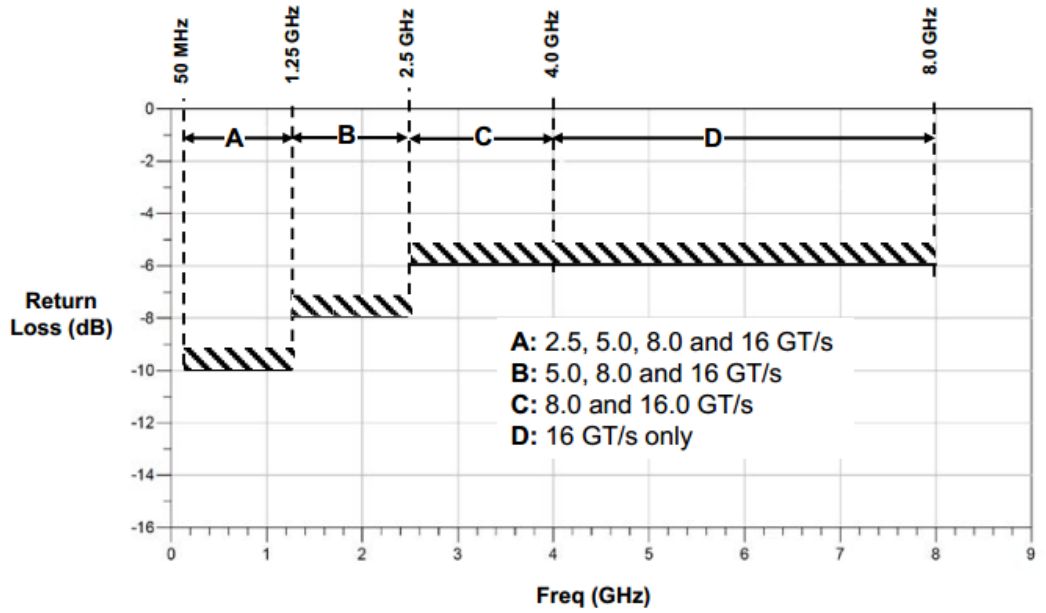



**Figure 8-19: Tx, Rx Differential Return Loss Mask**

# 技术特点

1.针对高速信号的设计：

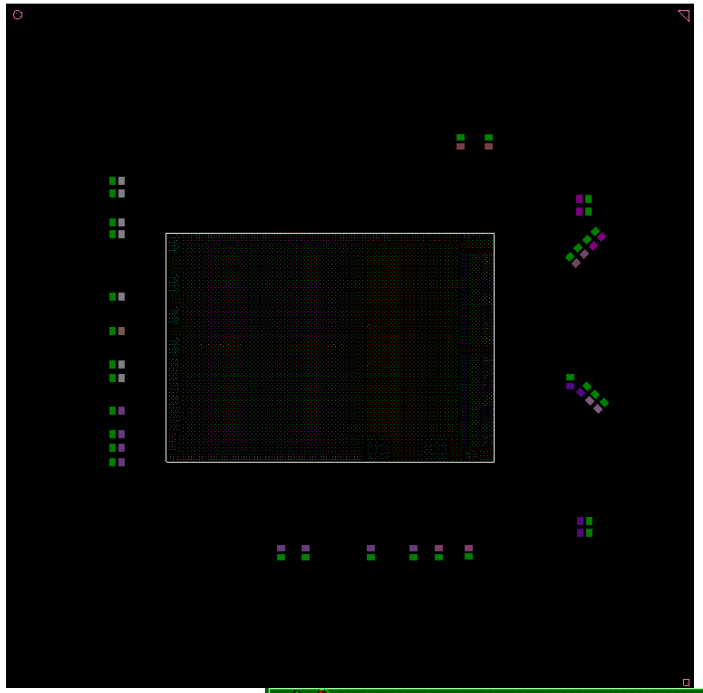
a)阻抗匹配；

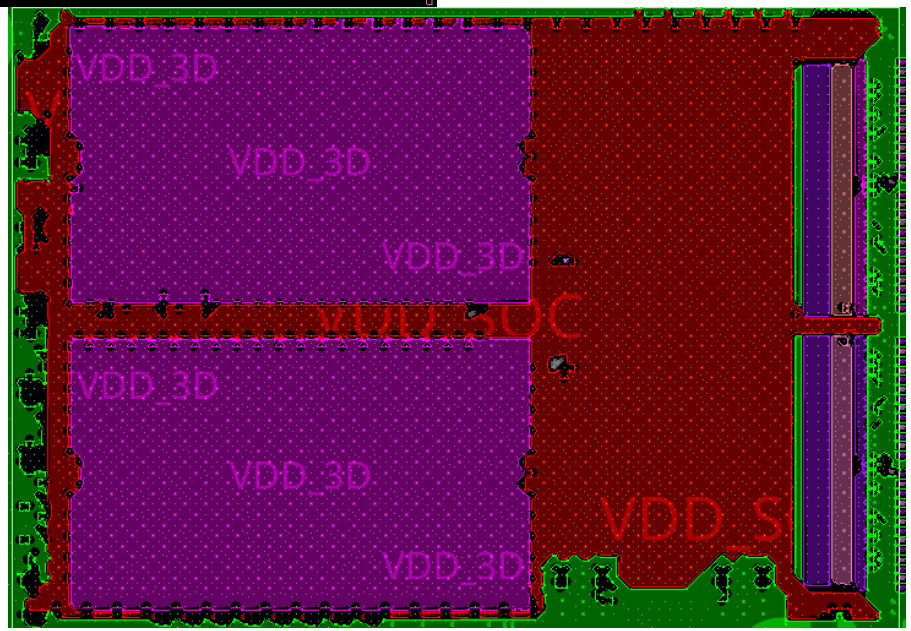
b)隔离度控制；

c)等长要求等；

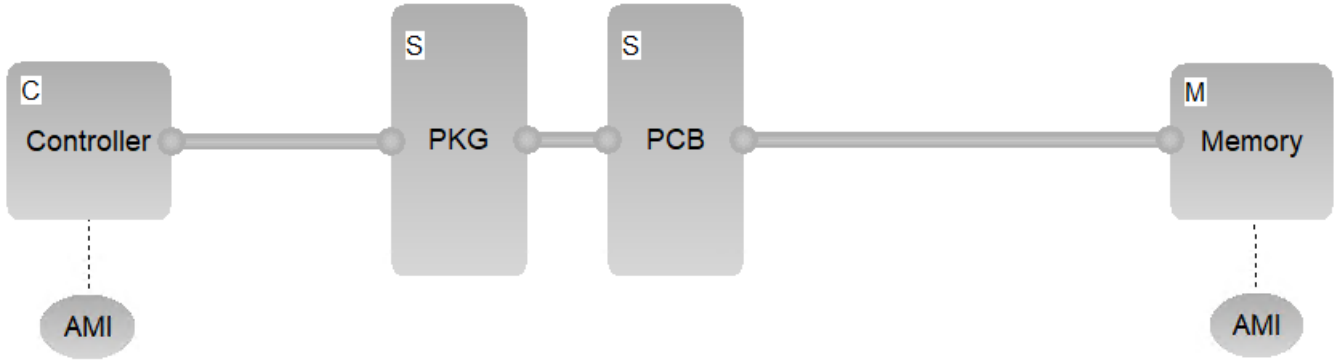
2.对于电源平面的最优化处理：完整的连接性

3.选择搭配电容容值和数量优化电源PI性能

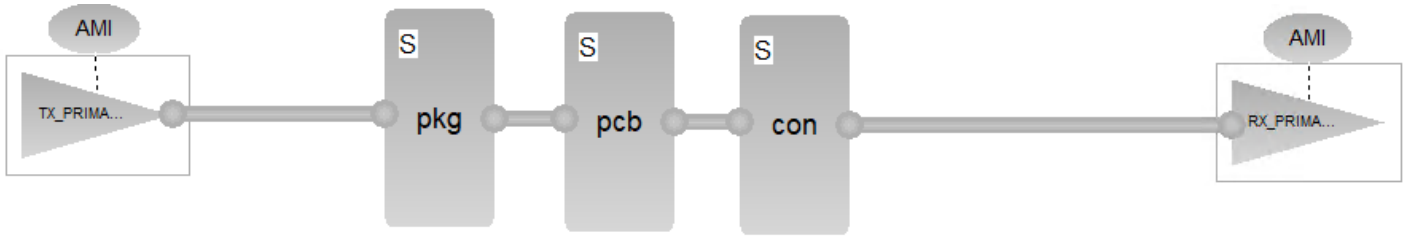




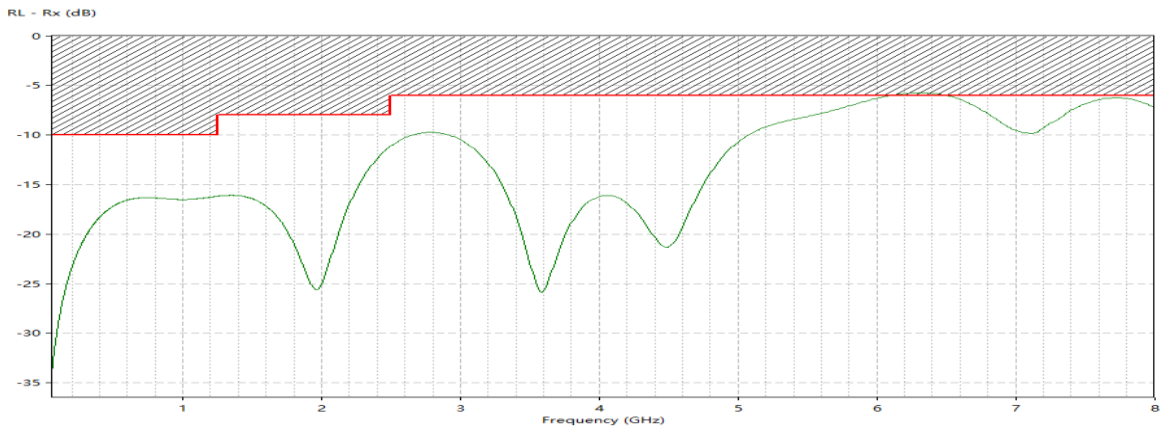
# 仿真结果

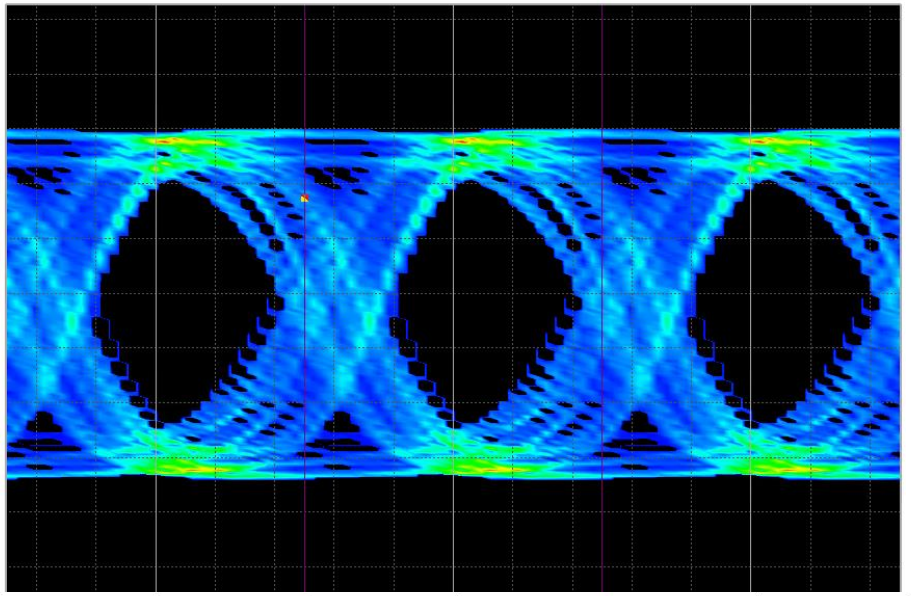


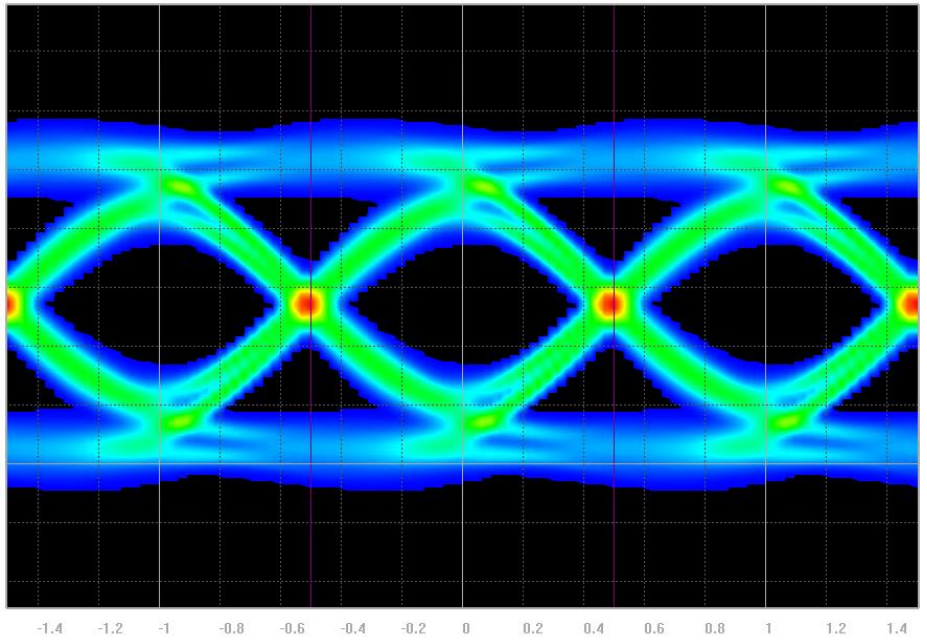

GDDR6 拓扑



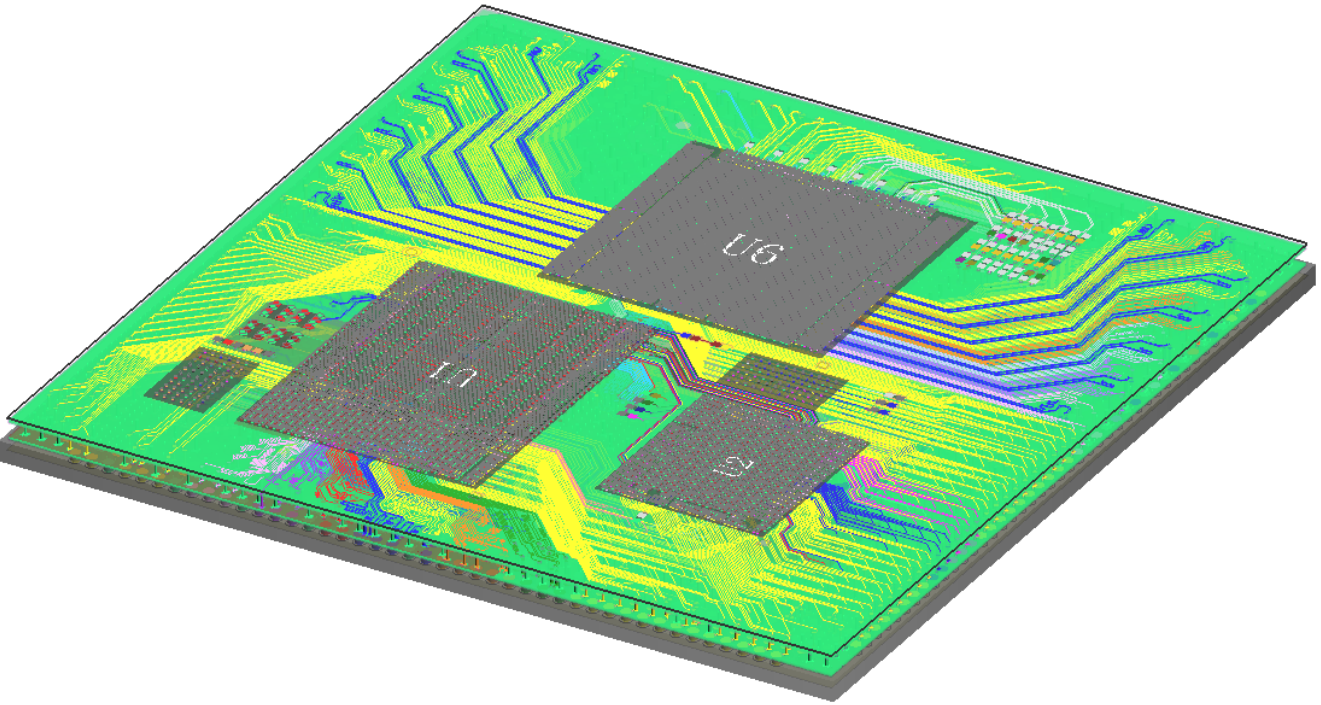

PCIe 拓扑





# SiP产品



应用领域：计算机微系统

| PKG Type | | FCBGA |
|---|---|---|
| PKG Size (mm) | | 50x50 |
| Die Size (mm) | | 17x16;14x19;11x10;3.6x6 |
| Die THK (um) | | 780 |
| Substrate | Layer / THK (mm) | 10L / 1.25 |
| | Core THK (um) | 820 |
| | PP THK (um) | 30 |
| | SR THK(um) | 25 |
| | Core Type | MCL-E705G |
| | PP Type | GZ41 |
| | SR Type | SR7300G |

# 主要参数

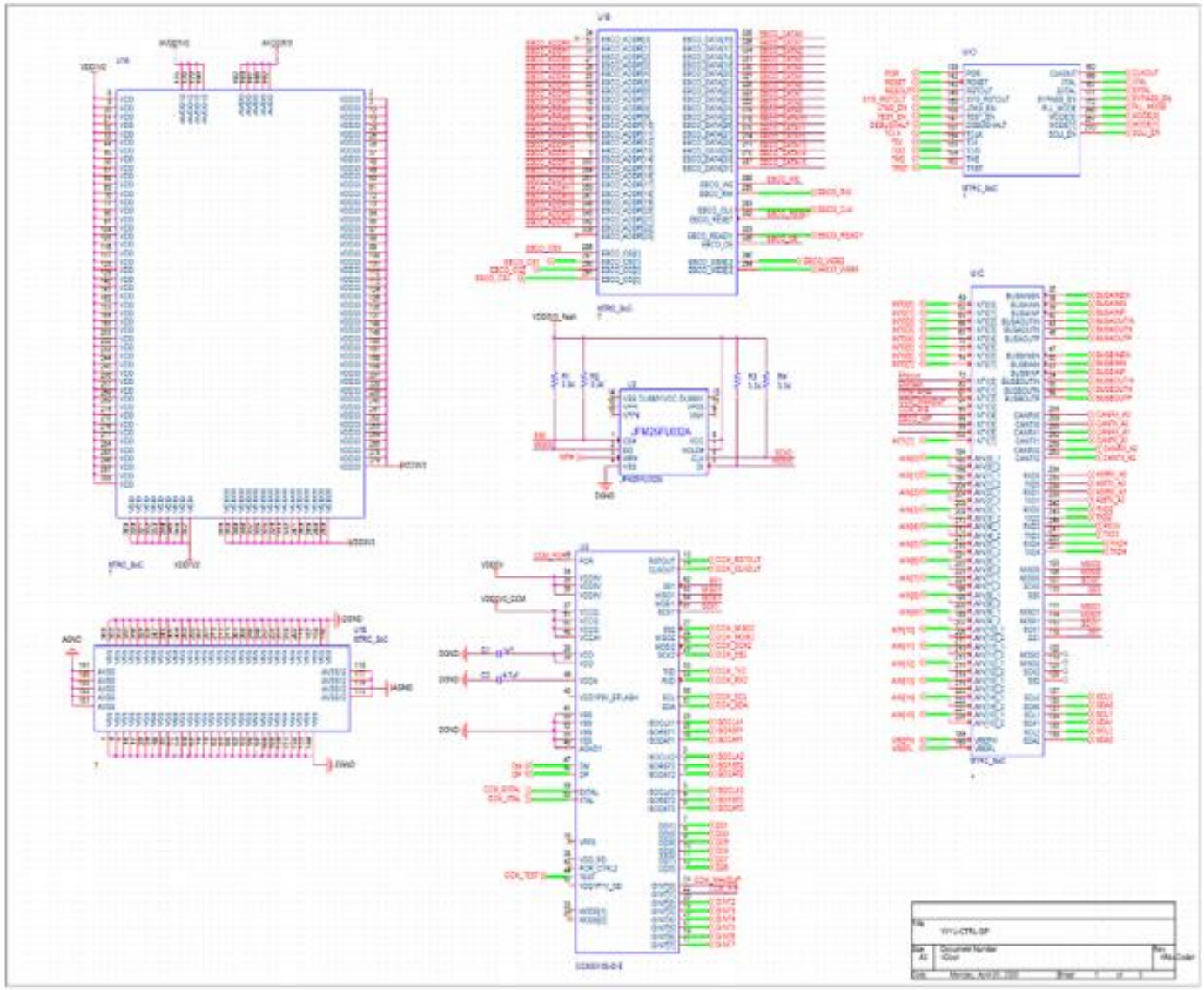
1.PCIe 3.0 8 Gbps

2. DDR3 2133Mbps

3.USB 2.0

4.VDD CORE:1V 40A

5. Power Dissipation: 50W+30W

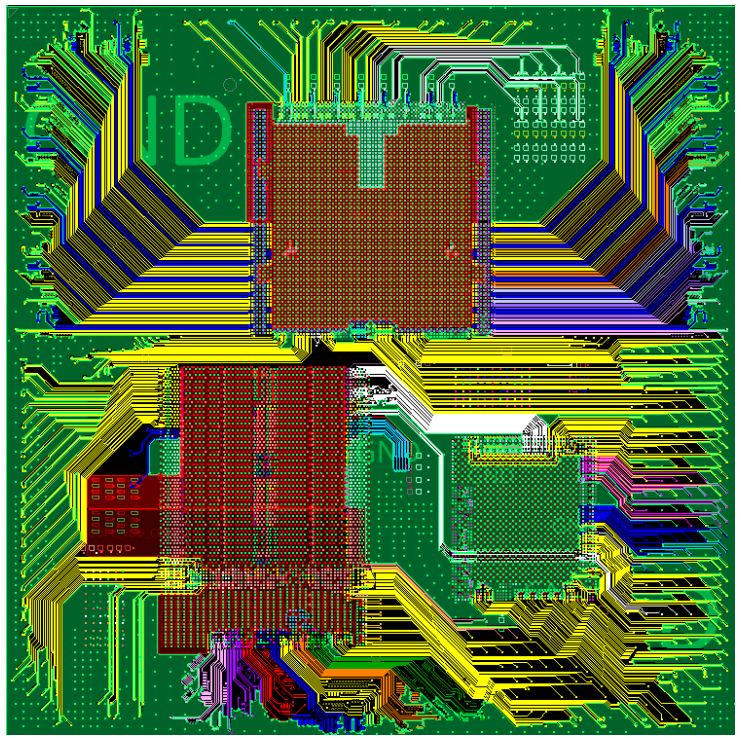


# 技术特点

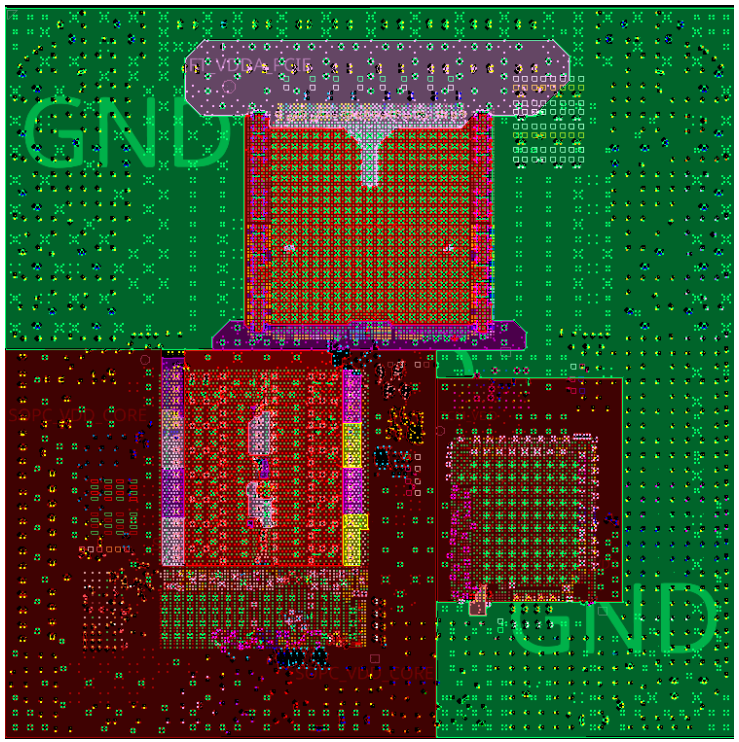
1.提供复杂芯片SiP原理图设计；

2.多芯片互连信号、电源连接性、完整性设计；

3.多芯片大尺寸封装翘曲控制（覆铜率：对称层<10%）

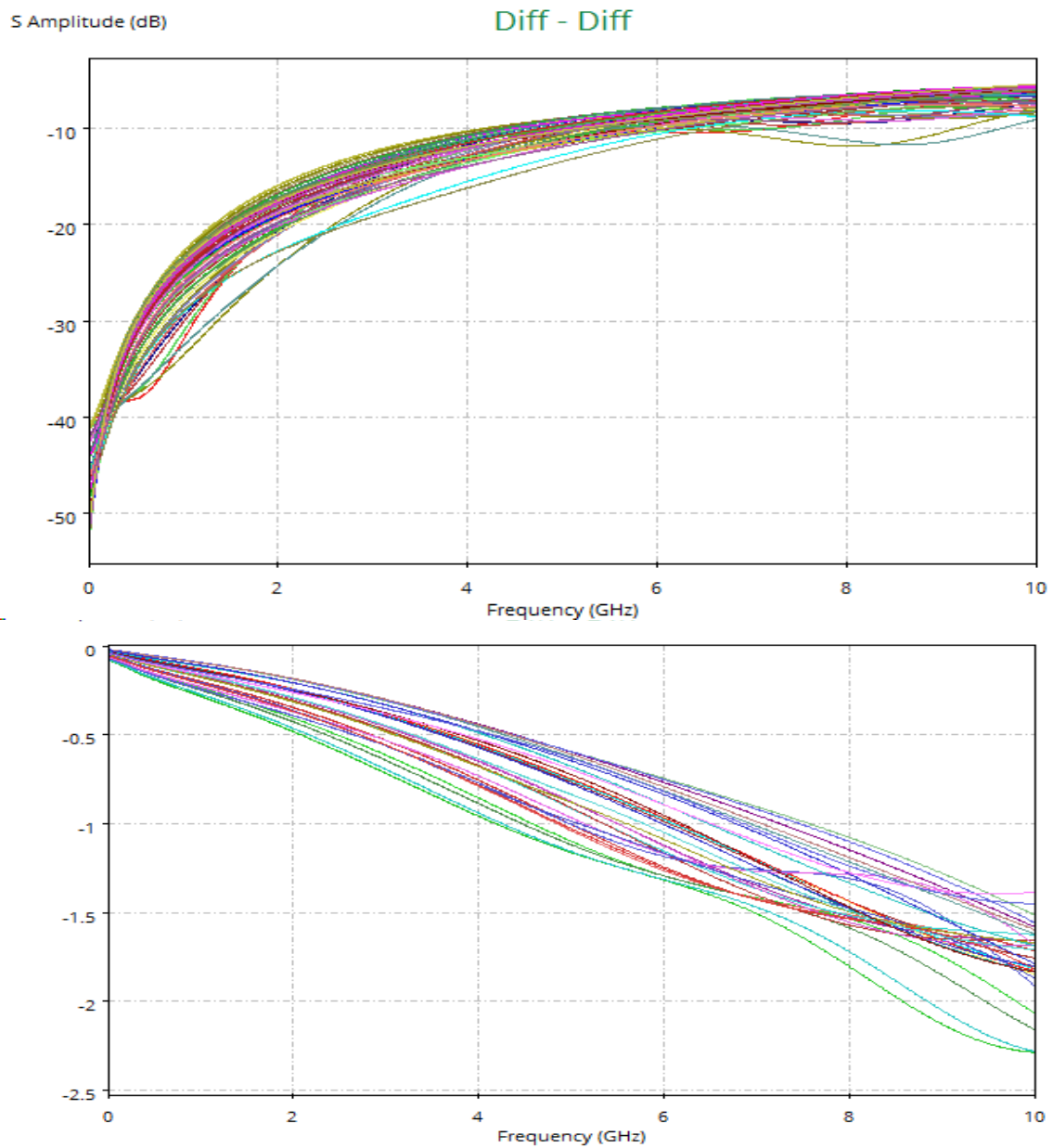


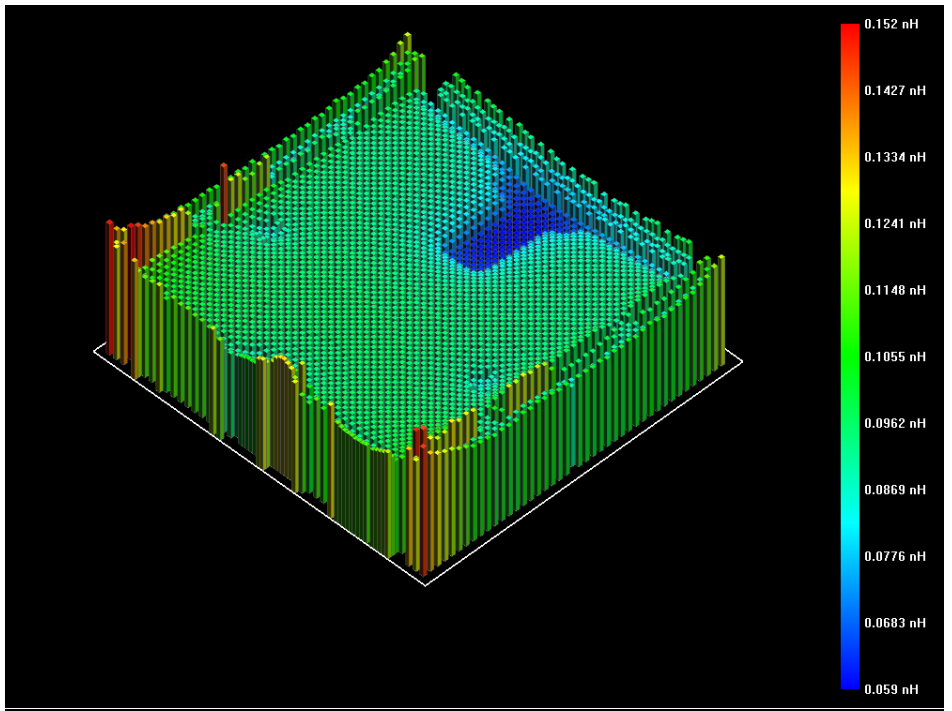
L2

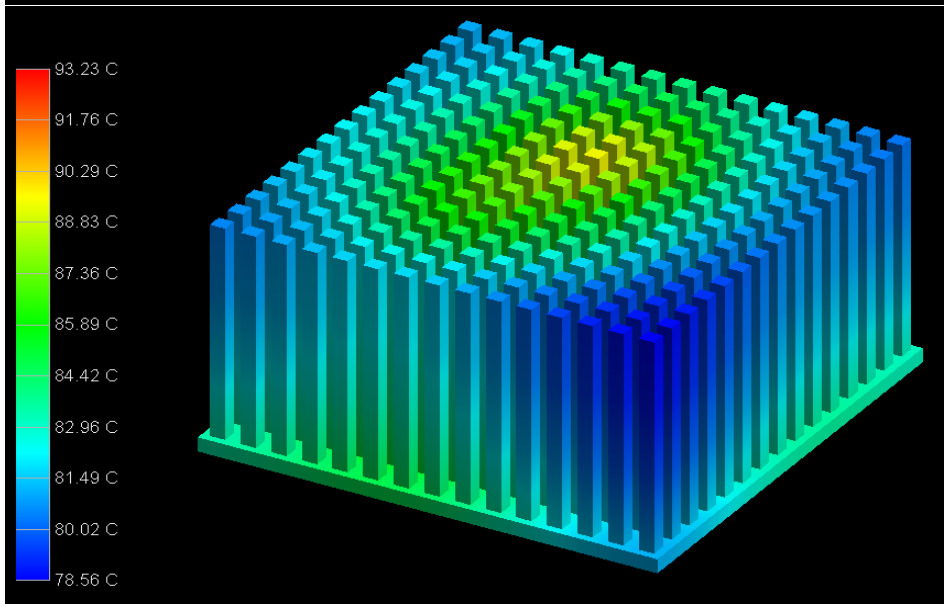



L6

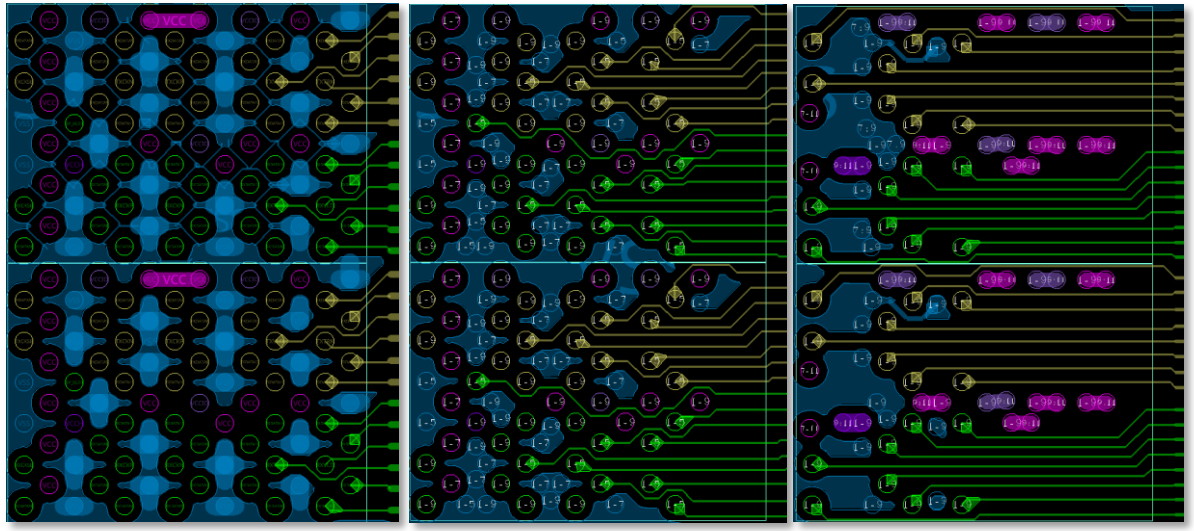
# 部分仿真结果


S Amplitude (dB)
Diff - Diff
-10
-20
-30
-40
-50
0
2
4
6
8
10
Frequency (GHz)
0
-0.5
-1
-1.5
-2
-2.5
0
2
4
6
8
10
Frequency (GHz)

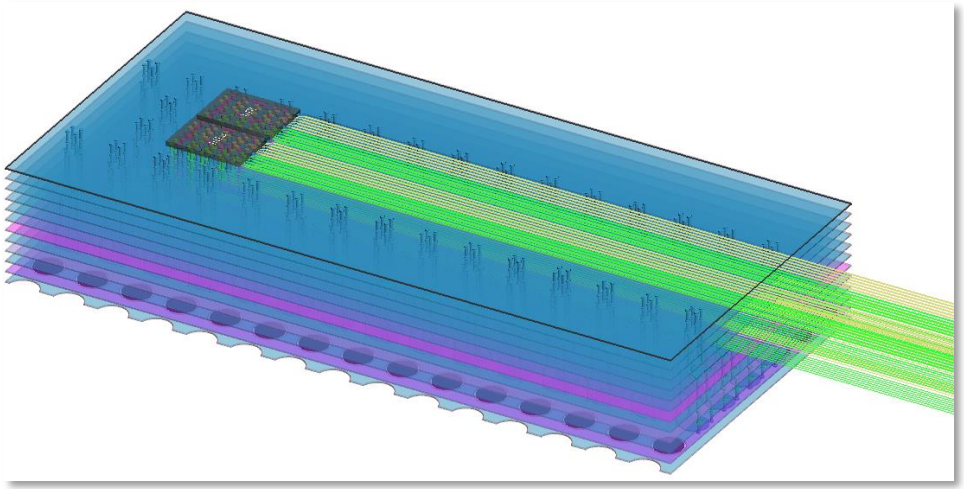

0.152 nH
0.1427 nH
0.1334 nH
0.1241 nH
0.1148 nH
0.1055 nH
0.0962 nH
0.0869 nH
0.0776 nH
0.0683 nH
0.059 nH


93.23 C
91.76 C
90.29 C
88.83 C
87.36 C
85.89 C
84.42 C
82.96 C
81.49 C
80.02 C
78.56 C

# UCIe D2D



Routing@L1 Routing@L3 Routing@L5



3D View

1. 5+2+5 Structure
2. Die size 12*16.5mm
3. Die to die 25mm
4. Route layer:1、3、5, refer to layer:2、4、6

**Design Purpose:**

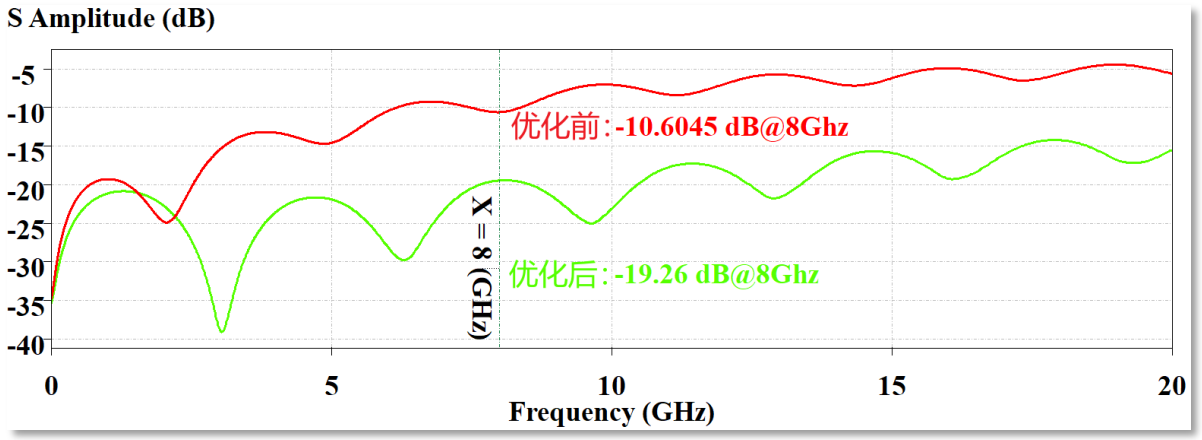
1, UCIe SP X16 sample substrate design SI/PI analysis(Data rate:16Gbps);
2, Compare IL and XTK with all options and meet UCIe standard requirement in 25mm.

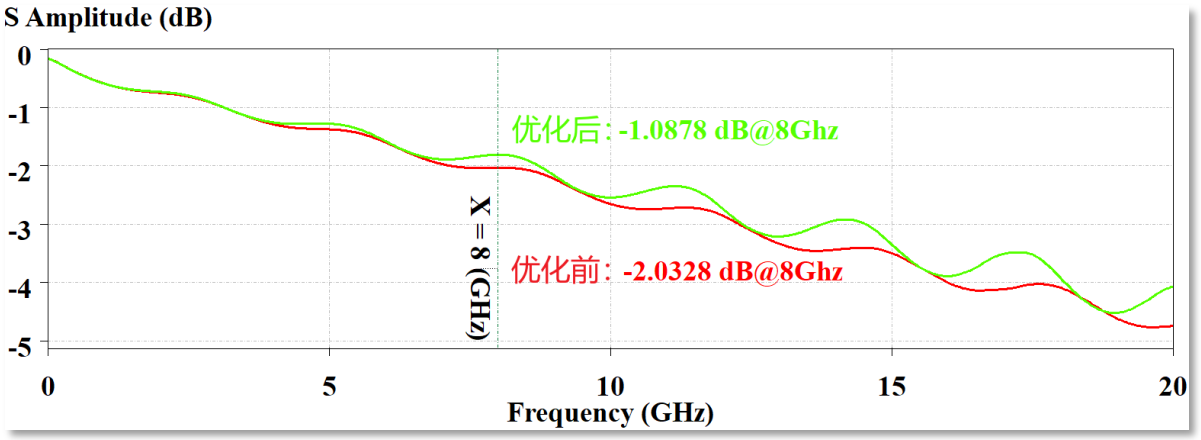
| Data Rate | 4-16Gb/s | 24-32Gb/s |
|---|---|---|
| Overall (Eye Closure due to Channel) | | |
| Eye Height | 40mV | 40mV |
| Eye Width (rectangular eye mask with specified eye height) | 0.75 UI | 0.65 UI with Equalization Enabled |

- 设计优化过程：
  --从平行线长度、出线端间距、蛇形绕线增加距离、信号之间隔地线、地过孔设计来优化串扰的影响。

| 方案# | 层数 | 信号走线层 | VSS参考层 | Die to Die | Single End Line (S/L/S) | Diff. Pair (S'/L/S/L/S') | Inside FC Line L/S | NET | S11 (dB) @8Ghz | S21(dB) @8Ghz | FEXT XTALK(dB) @8Ghz |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 方案一 | 10层 | 2、4 | 1、3、5 | 25mm | 40/18/40 um | 40/18/40/18/40um | 12/12 um | TX | -8 | -2.4 | -17 |
| | | | | | | | | RX | -8.5 | -2.4 | -19 |
| 方案二 | 10层 | 2、4 | 1、3、5 | 5mm | 40/18/40 um | 40/18/40/18/40um | 12/12 um | TX | -11 | -1.2 | -14.5 |
| | | | | | | | | RX | -10.5 | -1.1 | -16 |
| 方案三 | 12层 | 1、3、5 | 2、4、6 | 25mm | 100/18/100 um | 130/18/40/18/130um | 12/12 um | TX | -10.5 | -2 | -15 |
| | | | | | | | | RX | -9.5 | -2.2 | -19 |
| 方案四 | 12层 | 1、3、5 | 2、4、6 | 5mm | 100/18/100 um | 130/18/40/18/130um | 12/12 um | TX | -9.5 | -0.9 | -21 |
| | | | | | | | | RX | -9 | -1.4 | -16 |
| 方案五 | 12层 | 1、3、5 | 2、4、6 | 25mm | 100/18/100 um (在1/3/5层，分别选3根信号 | 130/18/40/18/130um | 12/12 um | TX | -10 | -2 | -23 |
| | | | | | | | | RX | -8 | -2.4 | -17.5 |
| 方案六 | 12层 | 1、3、5 | 2、4、6 | 25mm | 100/18/100 um(1/3/5部分线蛇形走线) | 130/18/40/18/130um | 12/12 um | TX | -9.5 | -0.9 | -21 |
| | | | | | | | | RX | -9 | -1.4 | -16 |
| 方案七 | 12层 | 1、3、5 | 2、4、6 | 25mm | 100/18/100 um(出线端拉开距离) | 130/18/40/18/130um | 12/12 um | TX | -10 | -2 | -23 |
| | | | | | | | | RX | -8 | -2.4 | -17.5 |
| 方案八 | 12层 | 1 | 2、4、6 | 25mm | 33/68 um | 18/40um | 15um | TX[0-15] | -13 | -1.5 | -24.6 |
| | | 3、5 | 2、4、6 | | 18/54um | | 12um | RX[0-15] | -14 | -1.5 | -22.7 |
| | | | | | | | | | | | RX13 -27 |
| | | | | | | | | | | | RX9 -23.5 |
| | | | | | | | | | | | RX8 -23 |
| 方案九 | 12层 | 1 | 2、4、6 | 25mm | 33/68 um | 18/40um | 11um | TX[0-15] | -18.5 | -1.7 | -26.5 |
| | | 3、5 | 2、4、6 | | 18/54um | | 12um | RX[0-15] | -18.5 | -1.7 | -25 |
| | | | | | | | | | | | RX13 -29 |
| | | | | | | | | | | | RX9 -26 |
| | | | | | | | | | | | RX8 -25 |
| 方案十 | 12层 | 1 | 2、4、6 | 25mm | 33/68 um | 18/40um | 12um | TX[0-15] | -19.5 | -1.78 | -27 |
| | | 3、5 | 2、4、6 | | 18/54um | | 12um | RX[0-15] | -19.5 | -1.78 | -27.5 |
| | | | | | | | | | | 1 | RX13 -30 |
| | | | | | | | | | | 3 | RX9 -36 |
| | | | | | | | | | | 5 | RX8 -30.6 |

# 仿真结果



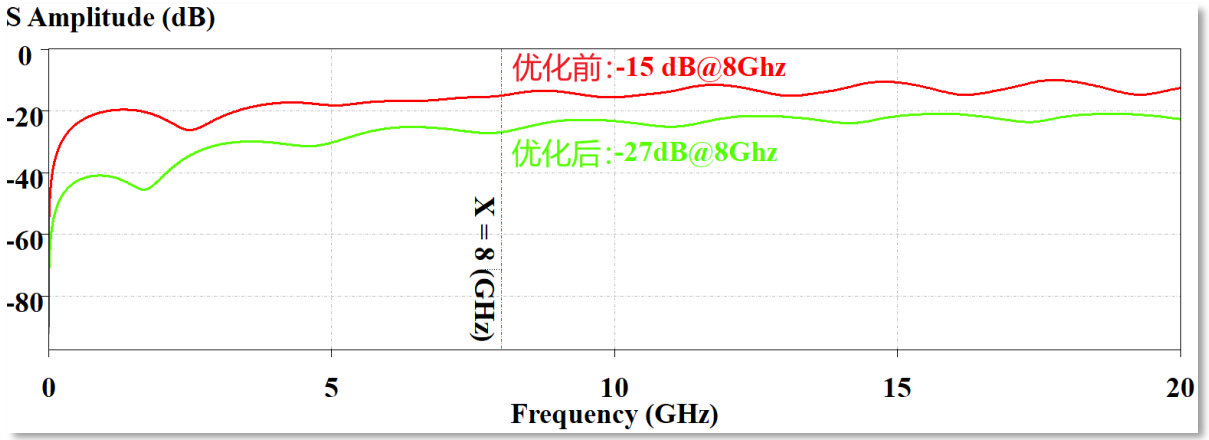
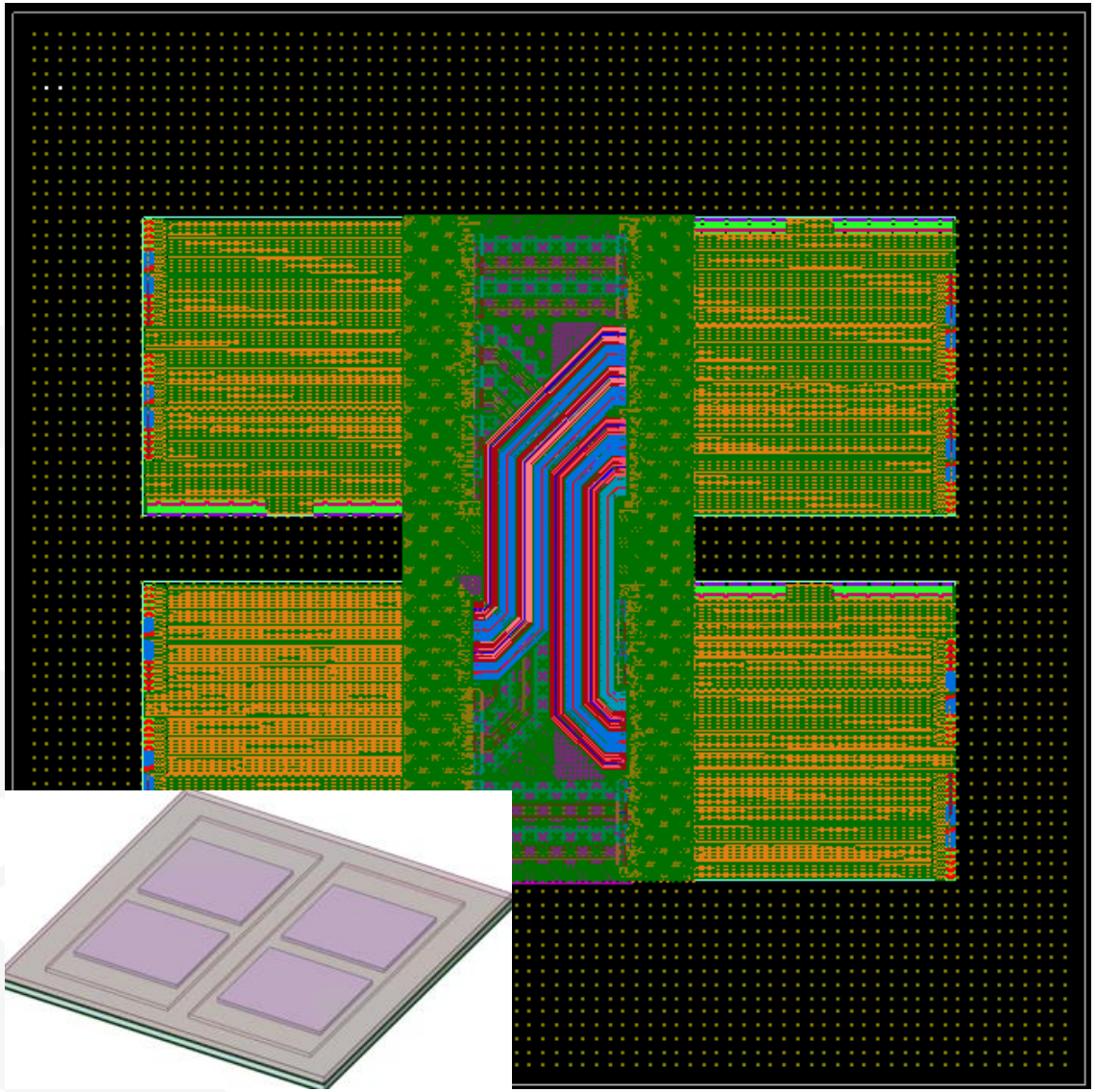



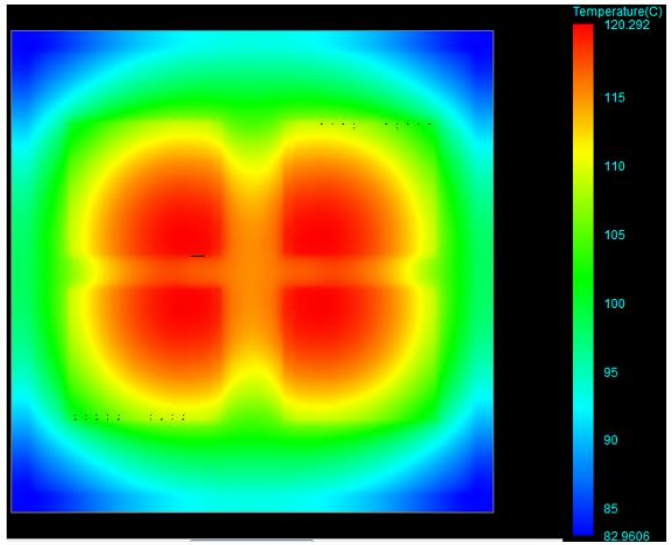

**Illustration note:**

Selected one of the key signals and display the comparison of S11 and S21 parameter curves before and after, as well as the comparison of crosstalk with adjacent lines.

# 定制化D2D 同构方案



➢ Temperature contours of Result（3D view）
环境温度25 ℃
环境空气流动速度：3 m/s

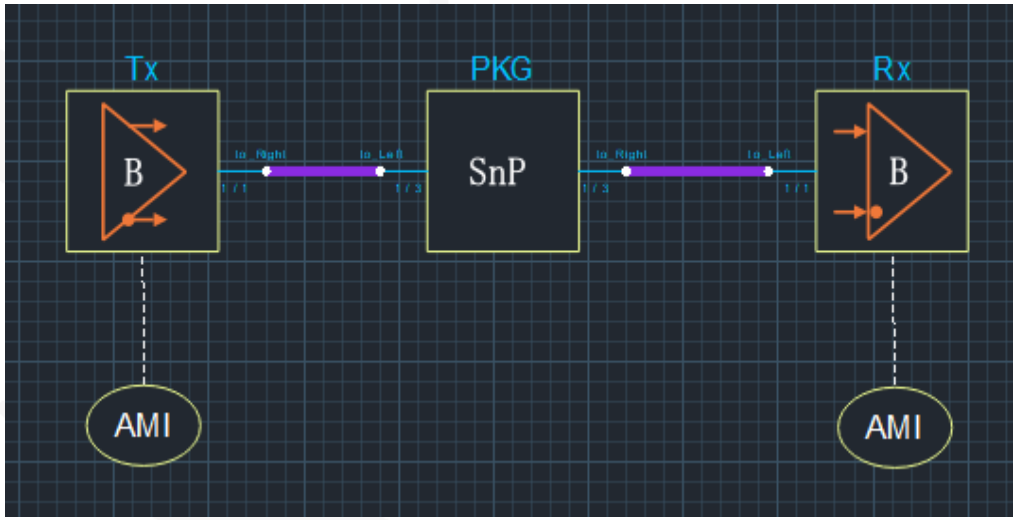


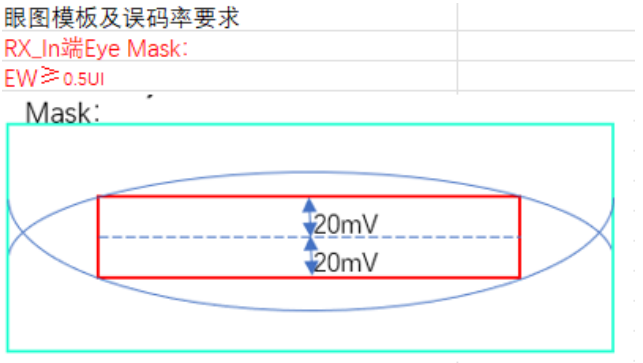

- 采用LpDDR5协议的 D2D高速互联 35bit x 8Gbps
- 产品尺寸80x80mm，基板叠层采用8+2+8结构，总厚度1.62mm；
- 四合一FC+散热盖子封装结构，芯片尺寸22.3x25.3mm；
- 主要信号线走2/4/6/8层，实现拓扑结构互连。
- PCIe5.0，LpDDR5等高速接口

# 技术参数

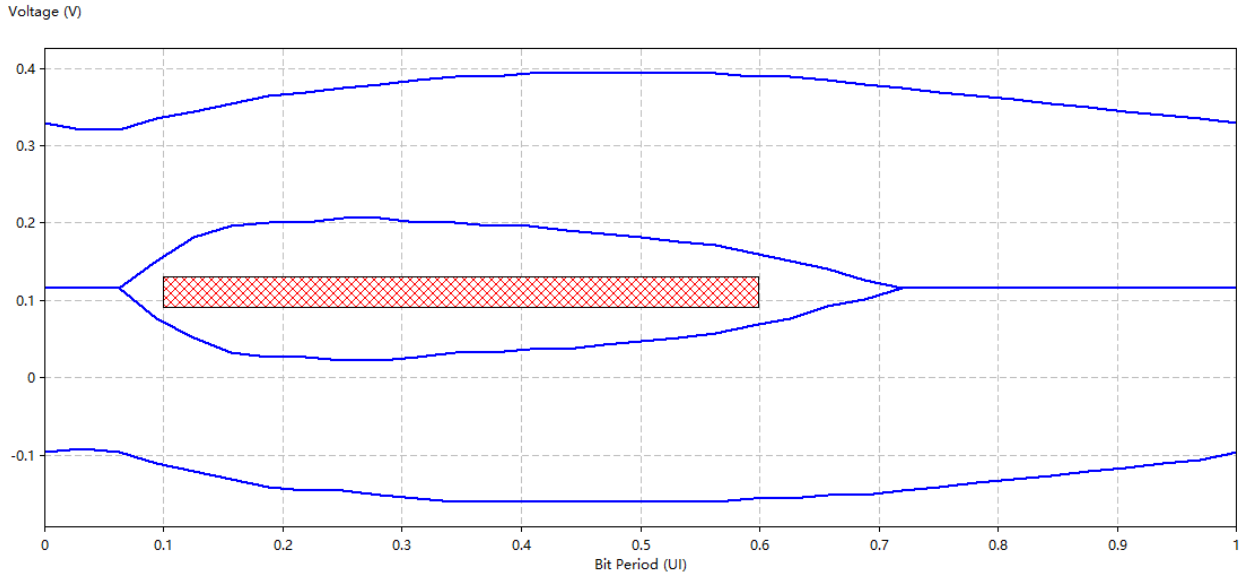
- D2D时域仿真设置：
  - 速率8Gbps
  - 码形：PRBS31
  - 拓扑结构如下图所示
  - Ideal power

D2D_TX_AMI\aks_d2dp_io_tx_ami.ibs



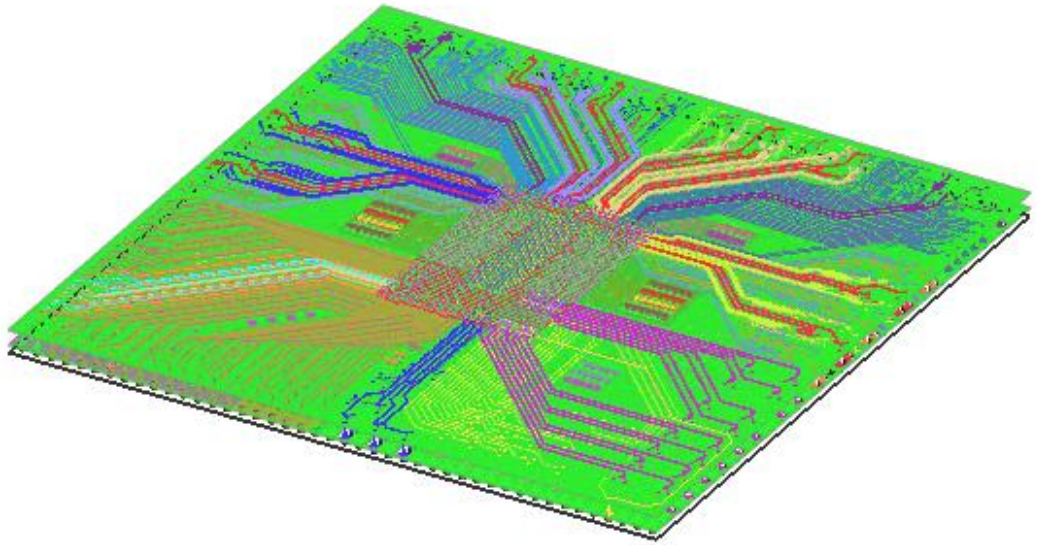




D2D_RX_AMI\aks_d2dp_io_Rtx_ami.ibs




红色方框按照模板0.5UI,40mV进行设置，眼图结果

# DPU产品



应用领域：DPU

| PKG Type | | FCBGA |
|---|---|---|
| PKG Size (mm) | | 45x45 |
| Die Size (mm) | | 10*15 |
| Die THK (um) | | 780 |
| Substrate | Layer / THK (mm) | 10L / 1.26 |
| | Core THK (um) | 820 |
| | PP THK (um) | 30 |
| | SR THK(um) | 20 |
| | Core Type | MCL-E705G |
| | PP Type | GZ41 |
| | SR Type | SR7300 |

# 主要参数

1.PCIE 4.0 x16 16Gbps

2.DDR4 x16 3200Mbps

3.ETH x4 10Gbps

4.Power Dissipation: 40W

| Category | Item | Targets |
|---|---|---|
| Impedance | TX / RX / CLK | 72.95~97.5ohm, suggest 85ohm |
| PKG | Skew within differential pair | <1ps |
| | Differential insertion loss | -1.5dB<8GHz |
| | Differential return loss | -15dB<8GHz, -10dB<16GHz |
| | Common mode return loss | -6dB<16GHz |
| | Common mode to differential mode conversion loss | -20dB<16GHz |
| | Differential to common mode conversion loss | -20dB<16GHz |
| | Differential crosstalk coupling (Near-end crosstalk between TX and RX at die side, all attackers) | -50dB<8GHz |
| | Differential crosstalk coupling (Far-end crosstalk between TX and TX, or RX and RX, all attackers) | -40dB<8GHz |
| Power | Vph | DC: 1%<br>AC: 3% |
| | Vp/VptxX/Vpdig | DC: 1%<br>AC: < 5% |
| Eye | width / height | 0.3UI / 15mV |

# 技术特点

1.PKG Dimension:50*50_12L→45*45_10L：成本↓

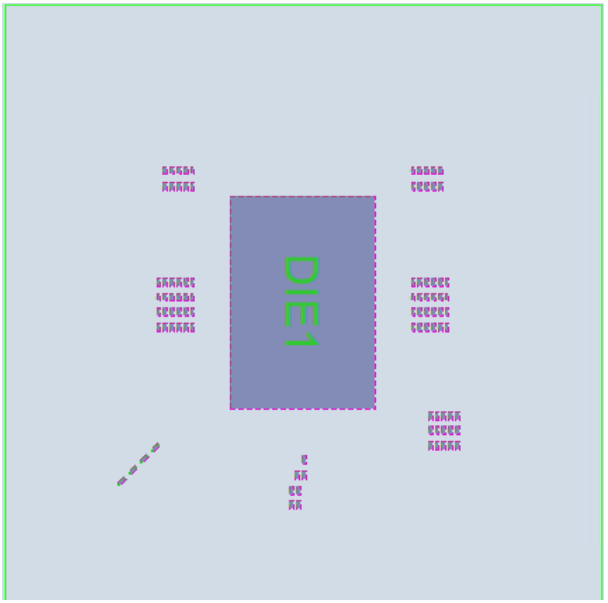
2.Dimension减少:布线层较少；电源层数减小

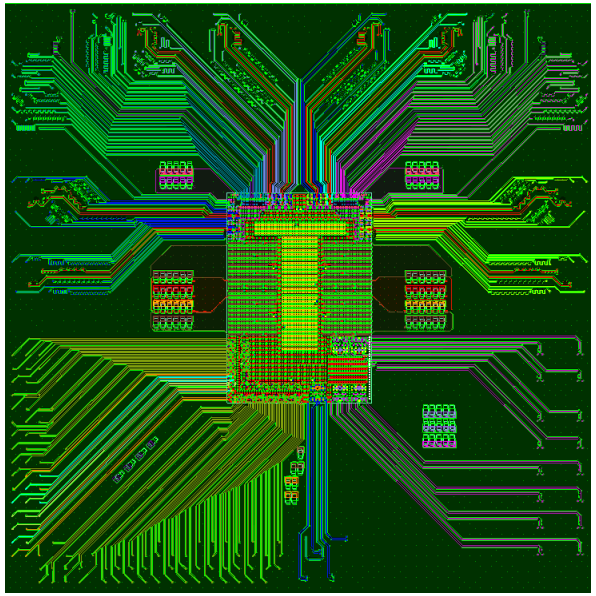
3.电容的选择和布局：

a) Core 上电源平面连接到电容；

b) 阶梯式电容值选择；

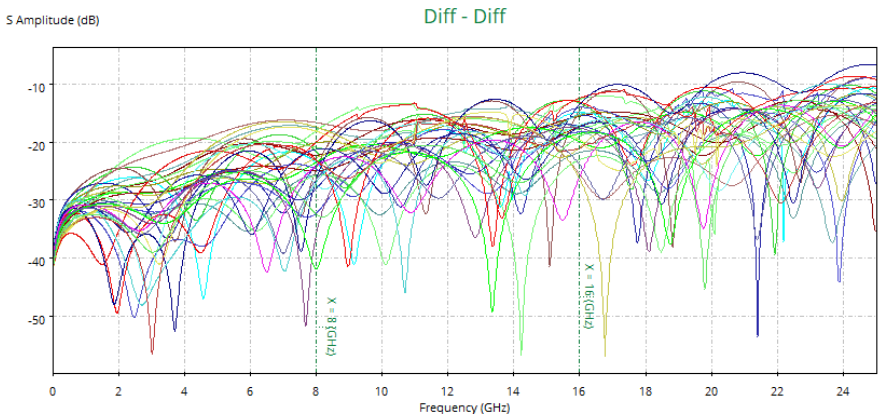
c) 对称电源拆分，保证PI满足要求。

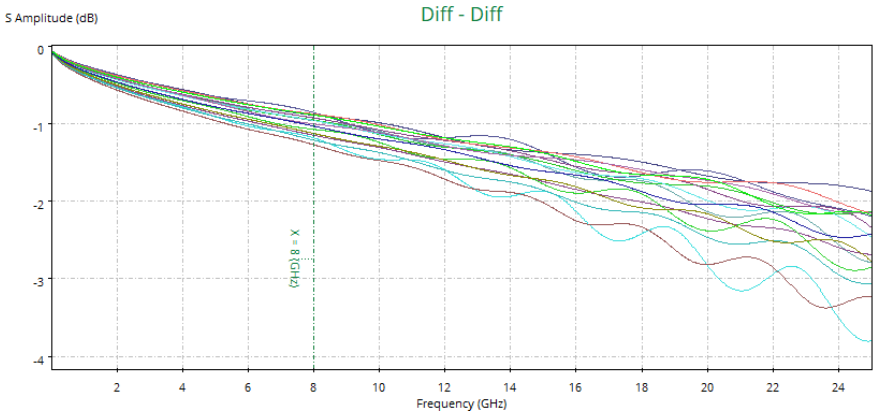


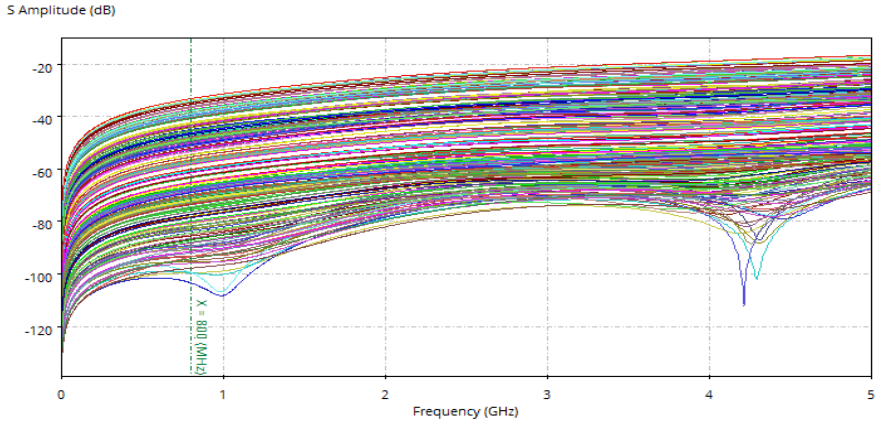



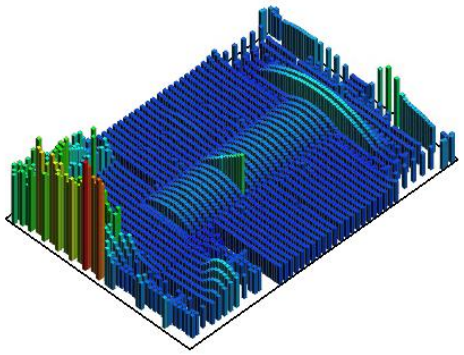
| 电容方案 | PDN(Ohm)@100Mhz |
|---|---|
| 无电容 | 3.62096E-02 |
| 2.2u x2/4.7u x3 | 2.58804E-02 |
| 10p/22n/2.2u x3 | 2.50259E-02 |
| 10p/22n/4.7u x3 | 2.45212E-02 |
| 10p/22n/2.2u/4.7u x2 | 2.36575E-02 |

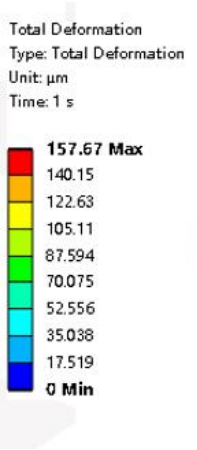
# 仿真结果

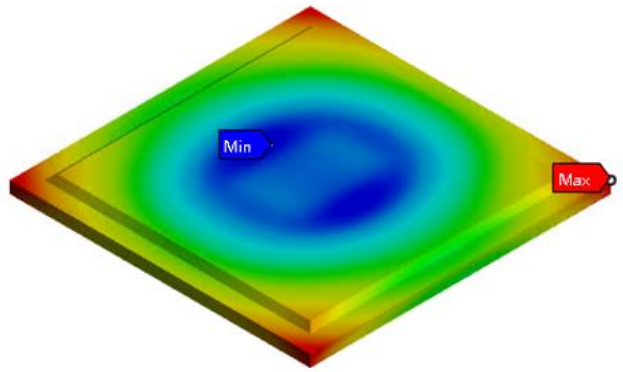


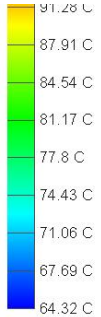



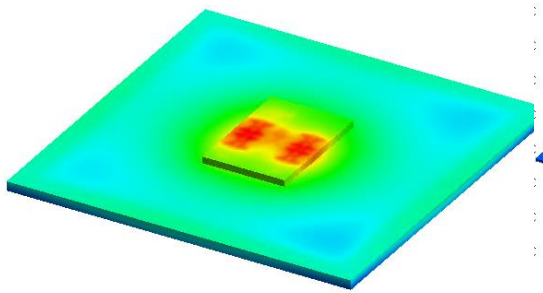



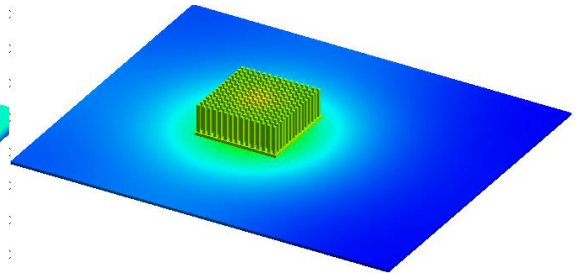



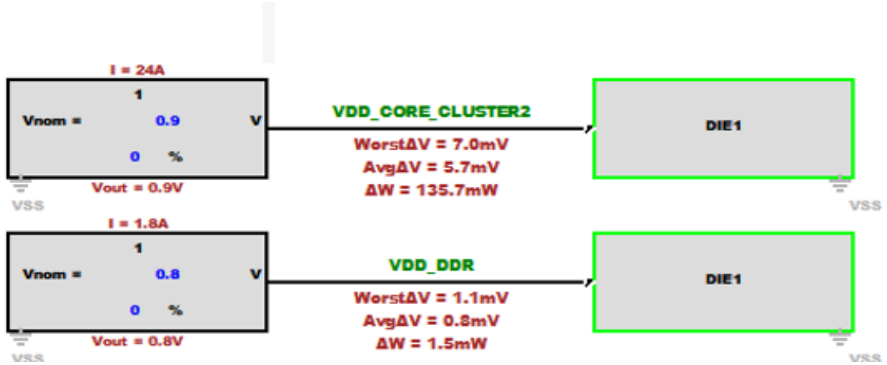



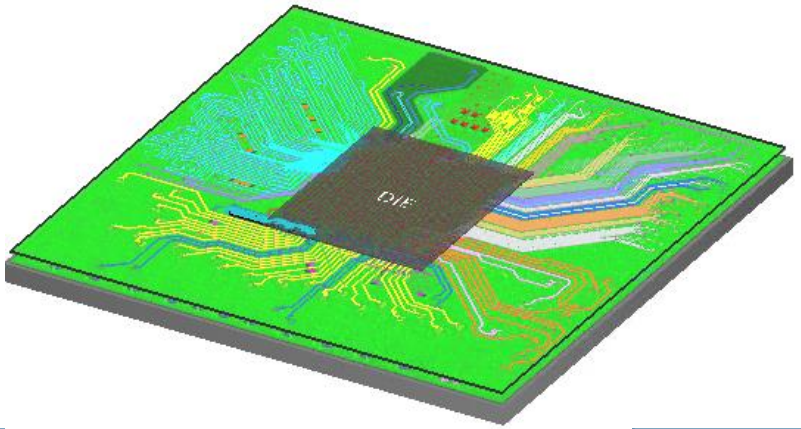








| | Actual Voltage(V) | Current(A) | IR Drop Simulated |
|---|---|---|---|
| VDD_CORE_CLUSTER2 | 0.892135 | 24 | ΔVp = 7.0mV(0.8%)<br>ΔVg = 0.9mV(<0.1%)<br>ΔV = 7.9mV(0.9%) |
| VDD_DDR | 0.79798 | 1.8 | ΔVp = 1.1mV(0.1%)<br>ΔVg = 0.9mV(0.1%)<br>ΔV = 2.0mV(0.3%) |

# 交换芯片产品




应用领域：通信

| PKG Type | | FCBGA(Trial 1) |
|---|---|---|
| PKG Size (mm) | | 31*31 |
| Die Size (mm) | | 12x10 |
| Die THK (um) | | 780 |
| Substrate | Layer / THK (mm) | 8L / 1.18 |
| | Core THK (um) | 800 |
| | PP THK (um) | 30 |
| | SR THK(um) | 25 |
| | Core Type | MCL-E705G |
| | PP Type | GZ41 |
| | SR Type | SR7300 |

| PKG Type | | FCBGA(Trail 2) |
|---|---|---|
| PKG Size (mm) | | 31*31 |
| Die Size (mm) | | 12x10 |
| Die THK (um) | | 780 |
| Substrate | Layer / THK (mm) | 6L / 1.08&0.67 |
| | Core THK (um) | 800(ABF)/400(BT) |
| | PP THK (um) | 30 |
| | SR THK(um) | 25 |
| | Core Type | MCL-E705G/832NS |
| | PP Type | GZ41/830NS |
| | SR Type | SR7300/SR1 |

# 主要参数

1. 28.125Gbps Serdes*8

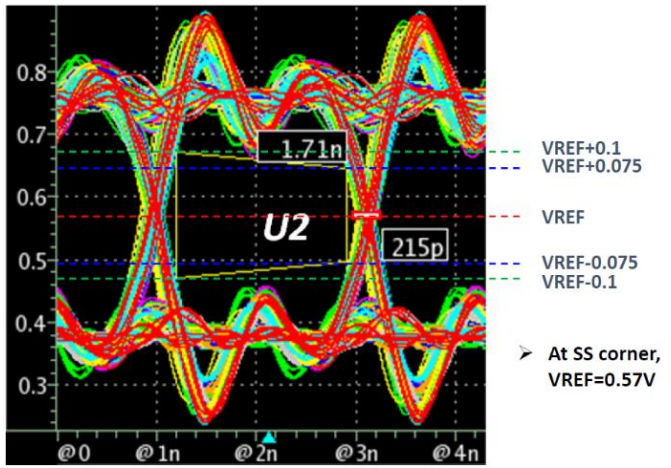
2. 12.5Gbps Serdes*24

2. DDR4 2400Mbps

3. Power Dissipation: 30W

| | | |
|---|---|---|
| 25G Serdes | Both TX and RX IL on pkg | <2dB@14 GHz; |
| | TX & RX PKG + Die Differential Return Loss | OIF_25G_VSR : -15.0 dB @ 14 GHz; |
| | TX PKG + Die Common-Mode Return Loss | OIF_25G_VSR: -2.2 dB @ 14 GHz; |
| | RX PKG + Die Reflected Differential to Common Mode Conversion | OIF_25G_VSR : -10 dB @ 14 GHz |
| | PKG Crosstalk | Tx to Tx -45 dB @ 14 GHz |
| | | Rx to Rx -45 dB @ 14 GHz |
| | | Tx to Rx -55 dB @ 14 GHz |
| | | RefClk to Tx/Rx -65 dB @ 14GHz |
| | PKG Differential Impedance | 90 ohm ±10% @ Rising time=25 ps |
| | PKG TX / RX Intra Skew | 0.5 ps |

**Eye Mask for CA**




➢ At SS corner, VREF=0.57V

*Spec.: EW > 1.08ns (0.65UI)*
*CA timing is 2T*

# 技术特点

1.10 layers to  8 Layers

a) 28Gbps serdes@L2/L7

b) 12.5Gbps@L2/L7

c) DDR4@L1/L3

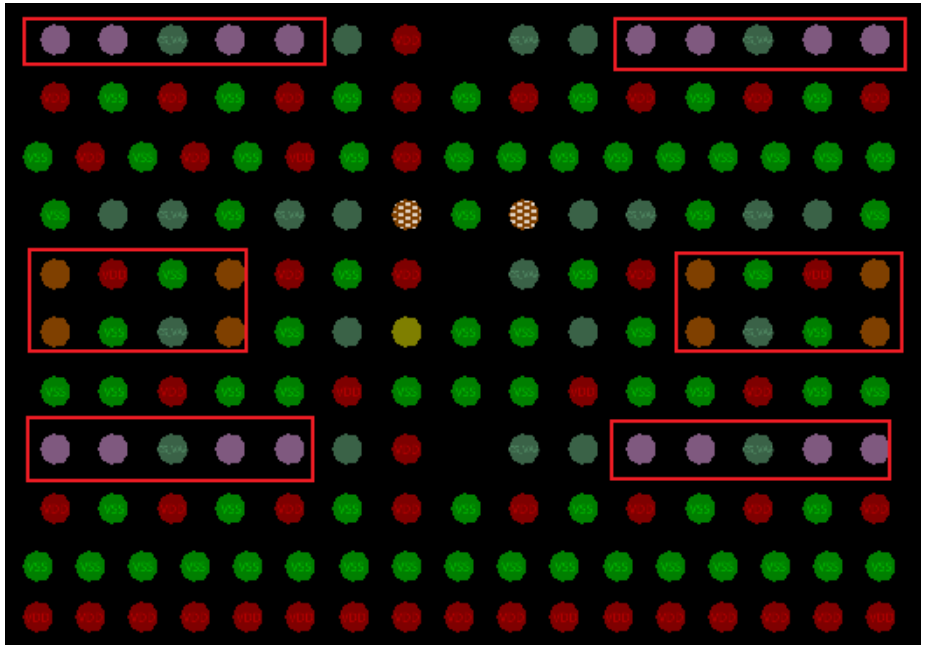
2.10 layers to  6 Layers (Delete 28Gbps Serdes)

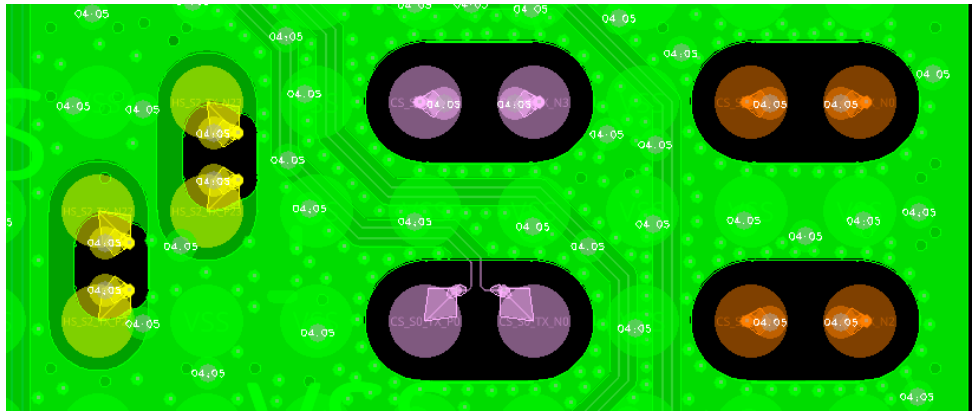
a) 12.5Gbps@L2/L7

b) DDR4@L1/L3

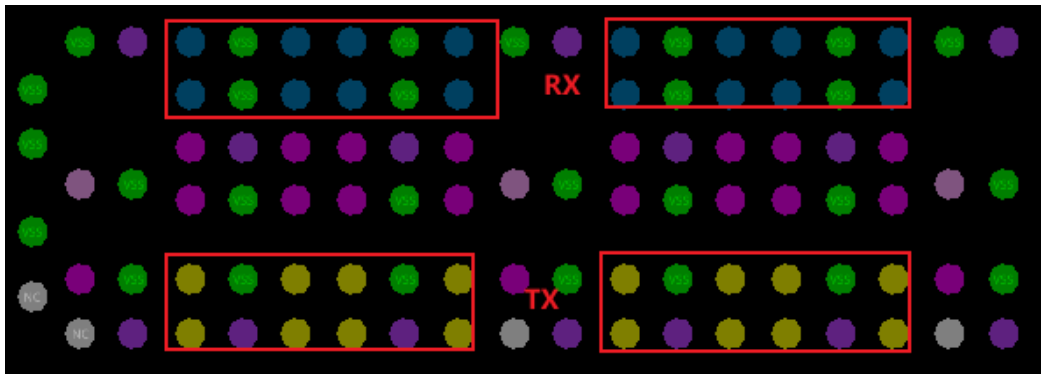
3.Void design for impedance match(Raise 5-10 ohm)

28Gbps Serdes

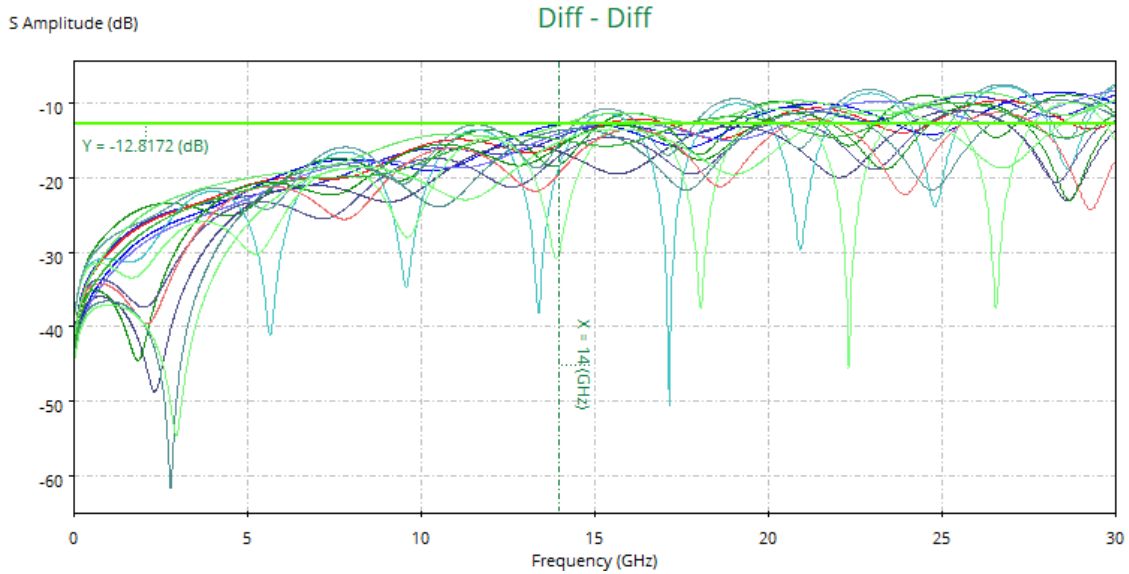


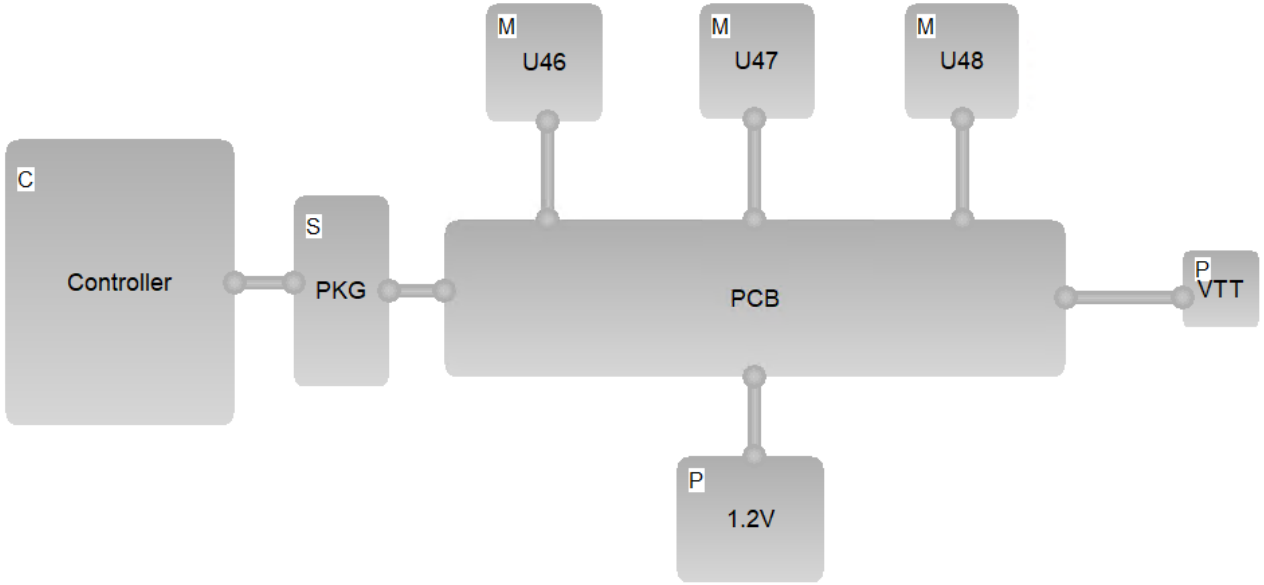


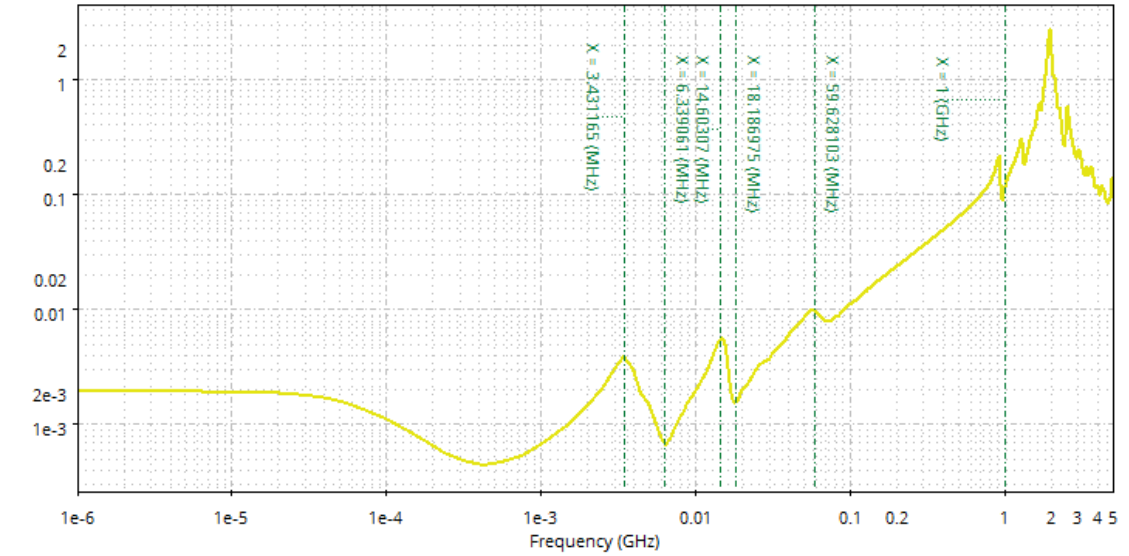
12.5Gbps Serdes

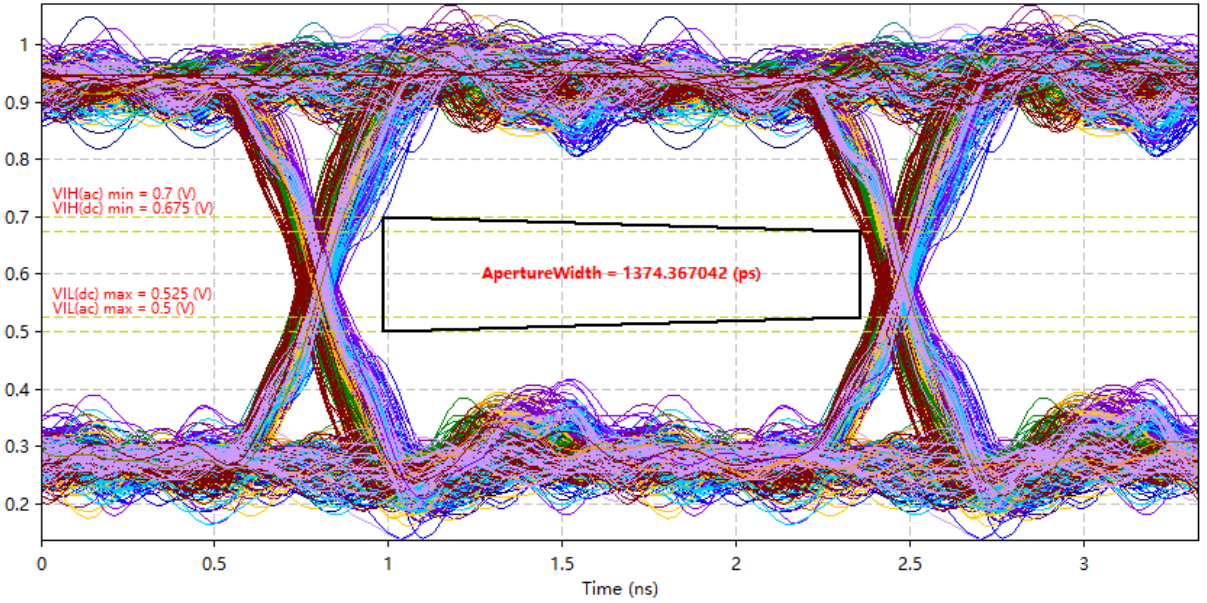


# 部分仿真结果


Diff - Diff
S Amplitude (dB)
Y = -12.8172 (dB)
X = 14 (GHz)
Frequency (GHz)


M
U46
M
U47
M
U48
C
Controller
S
PKG
PCB
P
VTT
P
1.2V

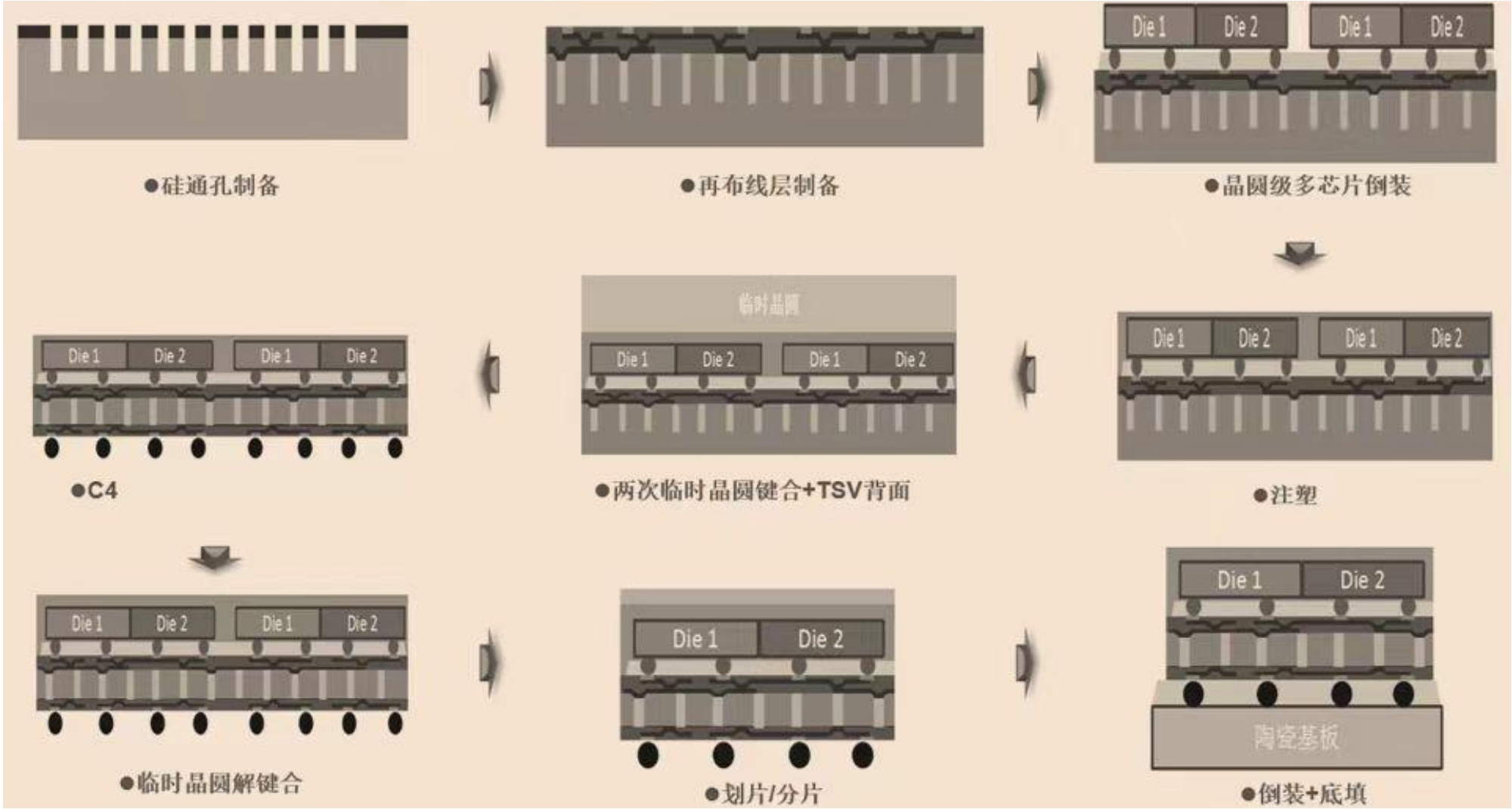

X = 3.431165 (MHz)
X = 6.339061 (MHz)
X = 14.60307 (MHz)
X = 18.186975 (MHz)
X = 59.628103 (MHz)
X = 1 (GHz)
Frequency (GHz)


VIH(ac) min = 0.7 (V)
VIH(dc) min = 0.675 (V)
VIL(dc) max = 0.525 (V)
VIL(ac) max = 0.5 (V)
ApertureWidth = 1374.367042 (ps)
Time (ns)


Chiplet（2.0D/2.5D）先进封装
锐杰微Chiplet D2D工作案例
锐杰微Chiplet工艺开发

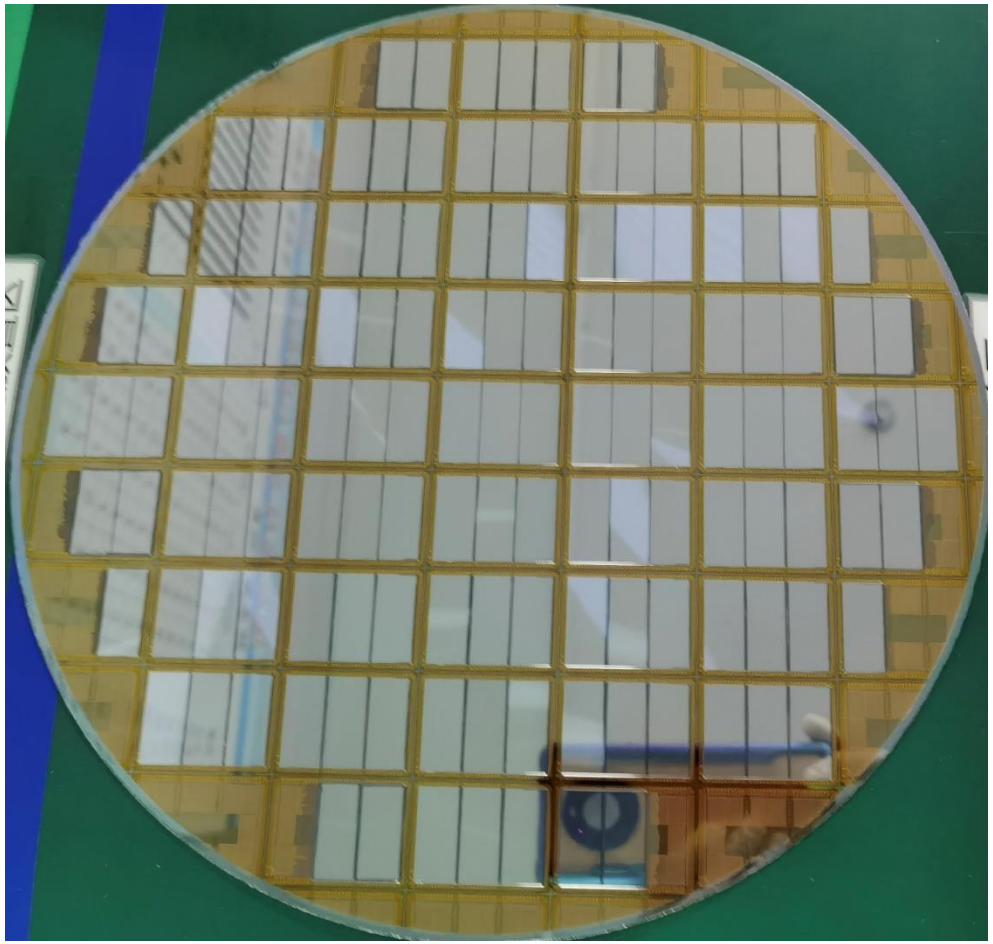
# ➢Chiplet 2.5D硅载板工艺

- 硅载板制作工艺(TSV+RDL)+封装



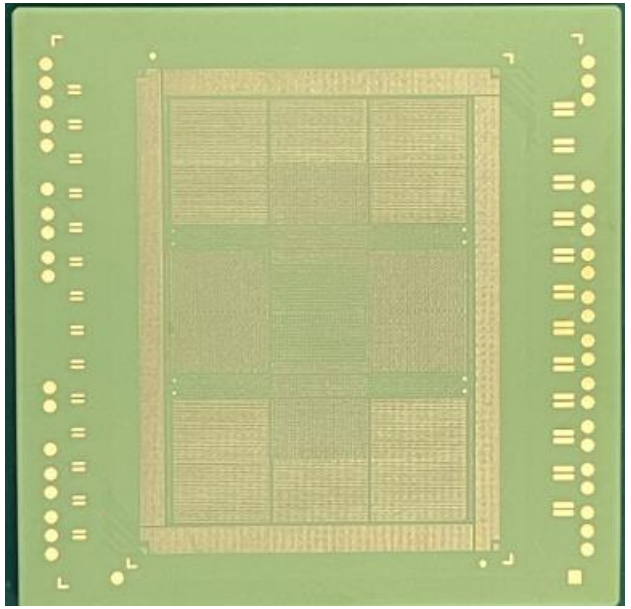
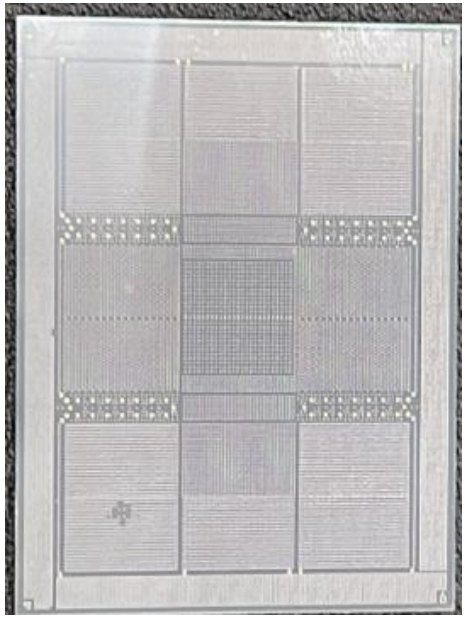
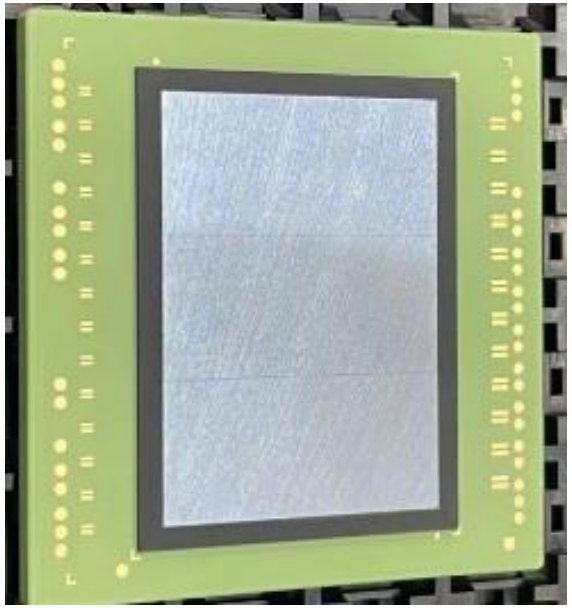
# ➢Chiplet 2.5D工艺研究

完成后的CoW

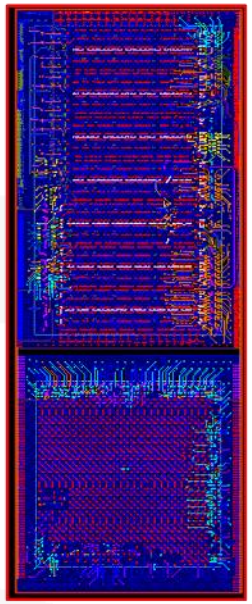


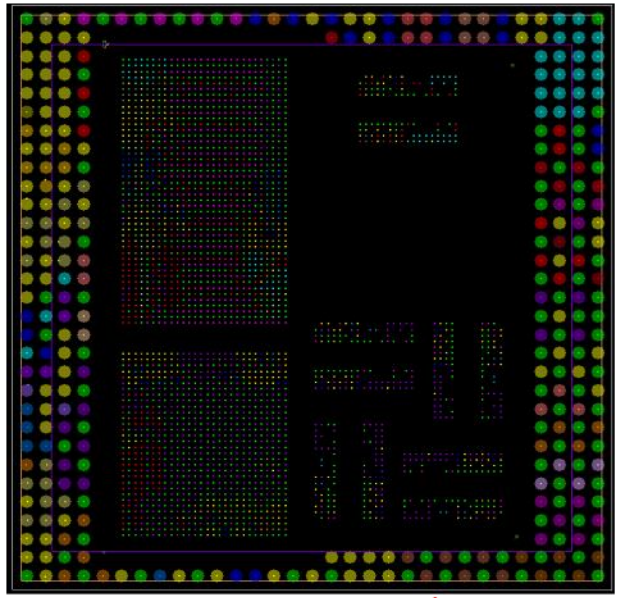
Si interposer size: 1.5x Reticle size
Die Bump pitch: 40um
Die Bump count: ~20000

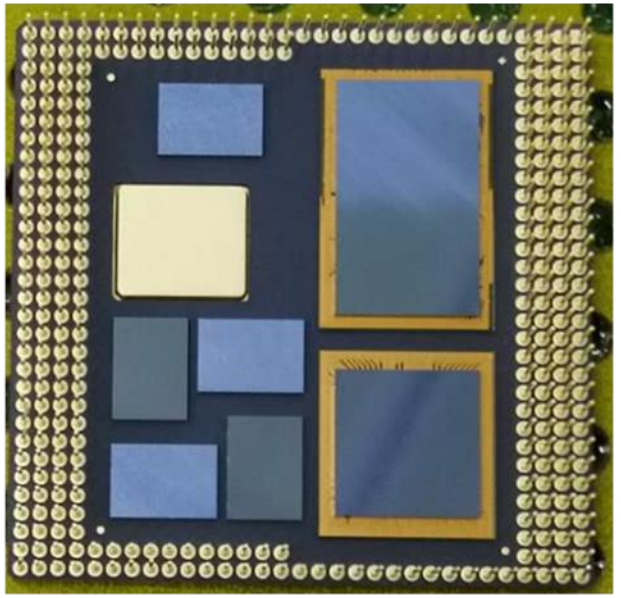
# Chiplet 2.5D工艺研究

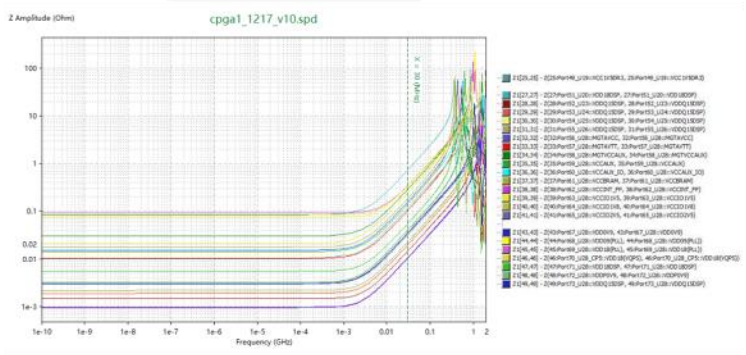




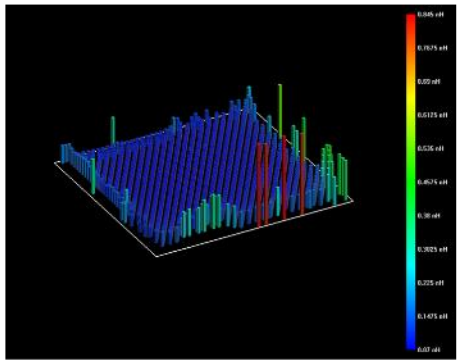

# TSV 2.5D转载板设计

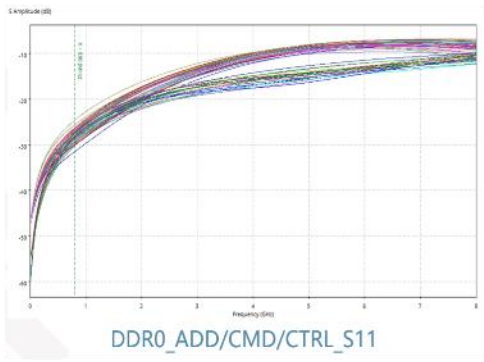


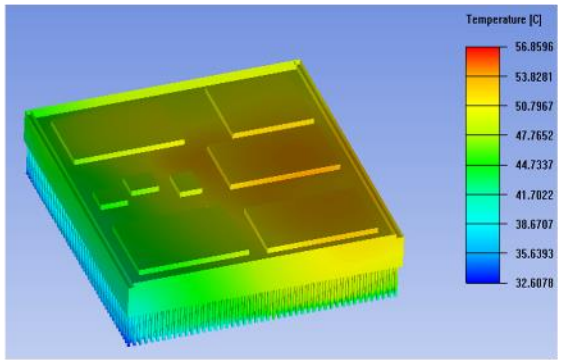






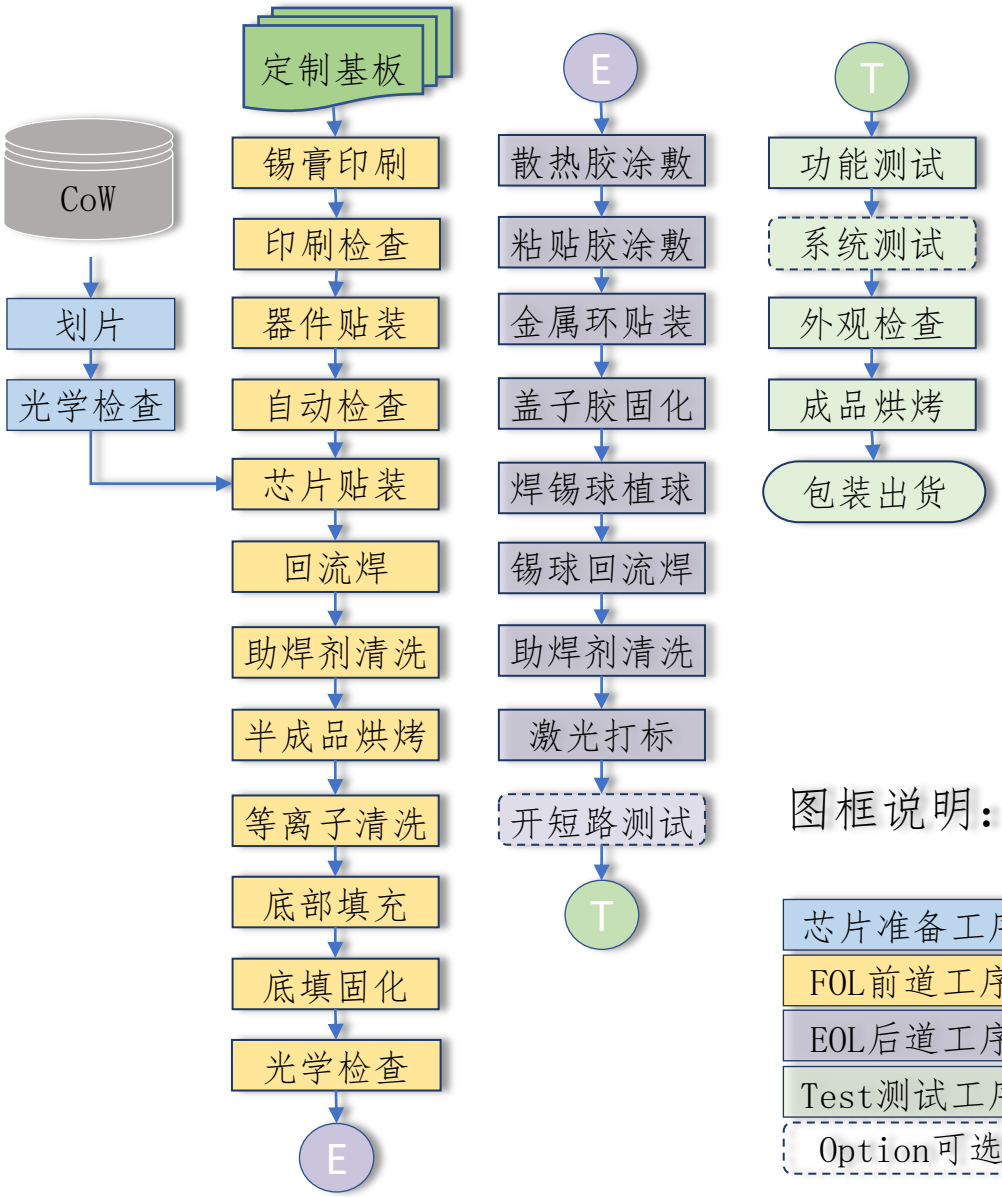





# ➢Chiplet 2.5D工艺-On Substrate工艺




图框说明：

- 芯片准备工序
- FOL前道工序
- EOL后道工序
- Test测试工序
- Option可选


# THANKS!