--第二届中国互连技术与产业大会

基于ADC/DSP的高速串行接口物理层的研究方法与关键技术

郑 旭 强

中国科学院微电子研究所

2022 .12 .16

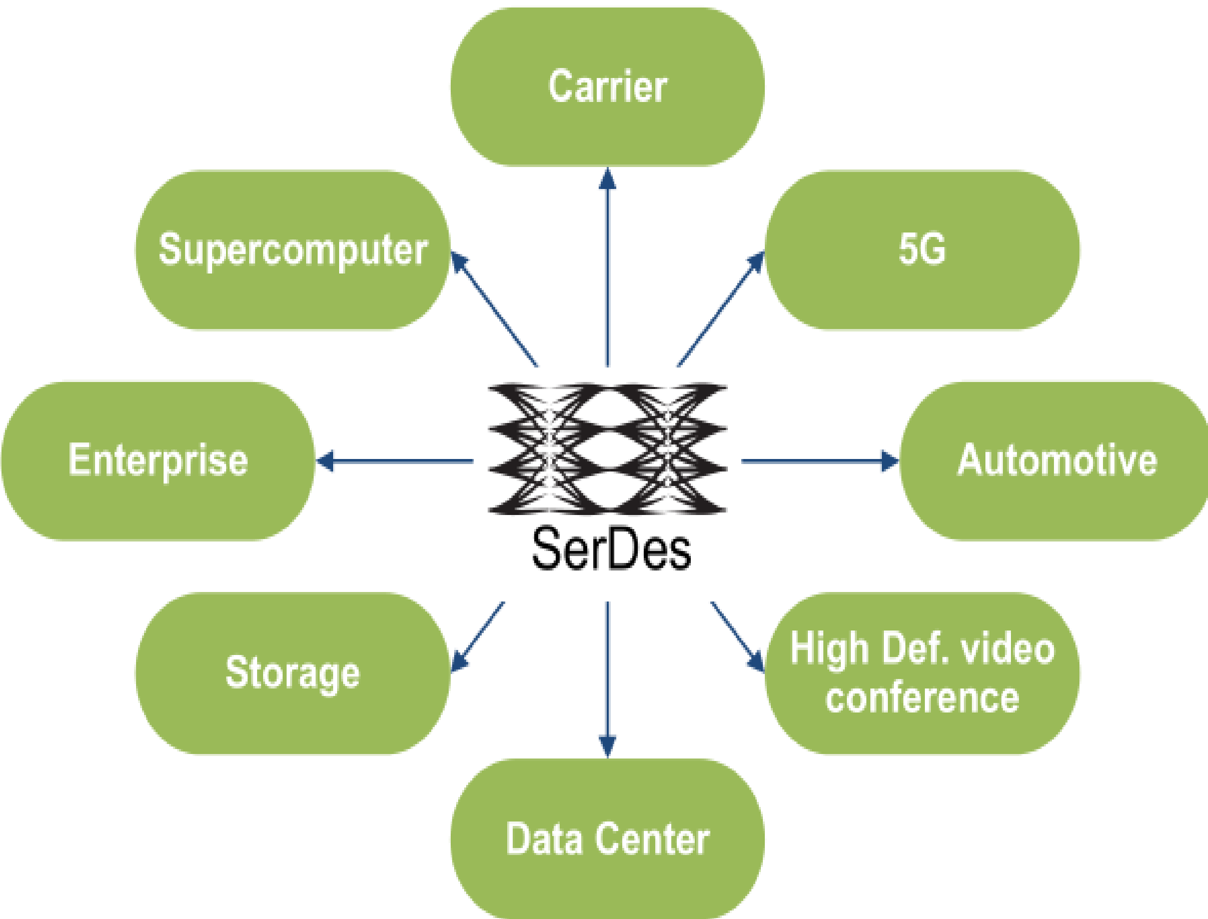
提 纲

- SerDes发展趋势与应用场景
- SerDes研究方法与关键技术
  - 系统级建模与仿真
  - 电路级技术演进
- 基于ADC/DSP PAM4 收发机

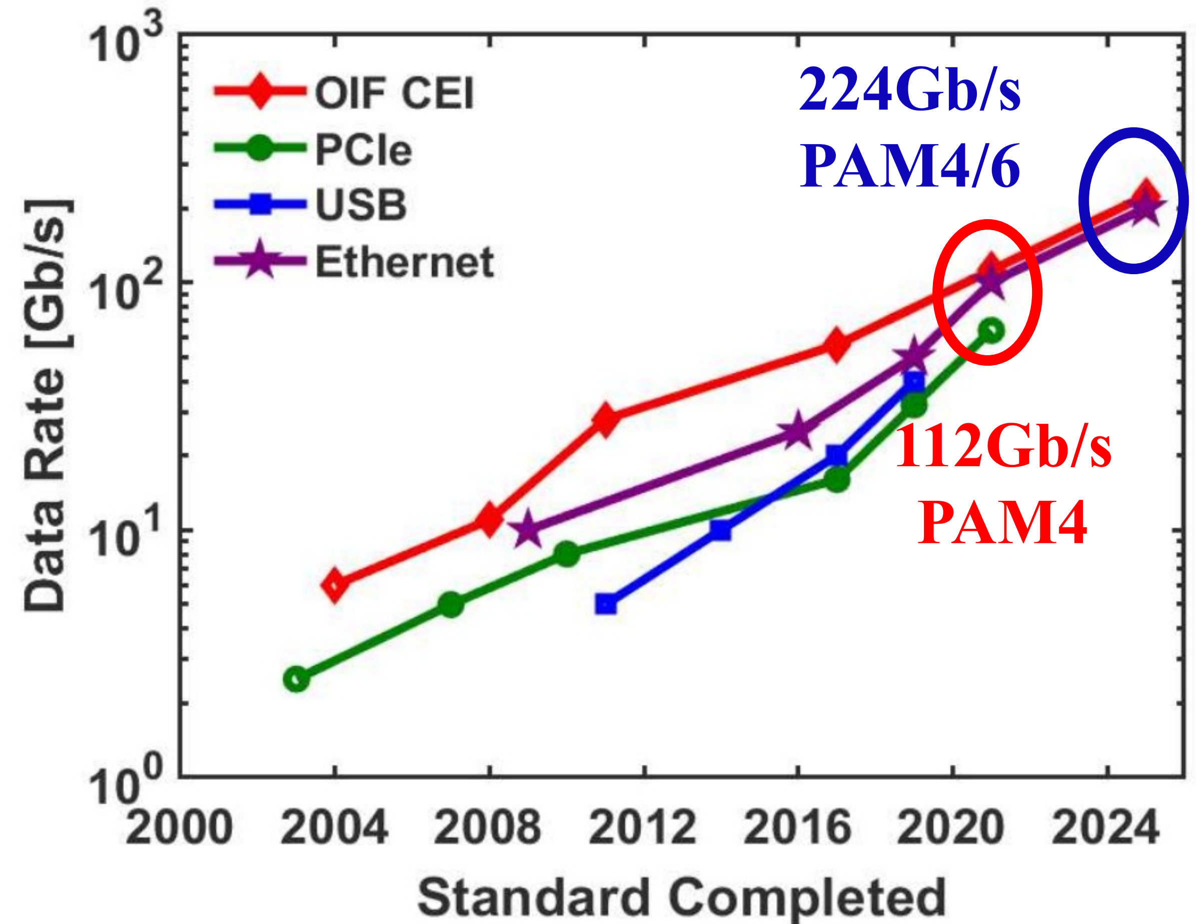
提 纲

- SerDes发展趋势与应用场景
- SerDes研究方法与关键技术
  - 系统级建模与仿真
  - 电路级技术演进
- 基于ADC/DSP PAM4 收发机

Background-Applications and Trends



Marvell，ISSCC2022



T. Musah, "Wireline Link Standard," [Online]. Available: https://mics.engineering.osu.edu/iostandards

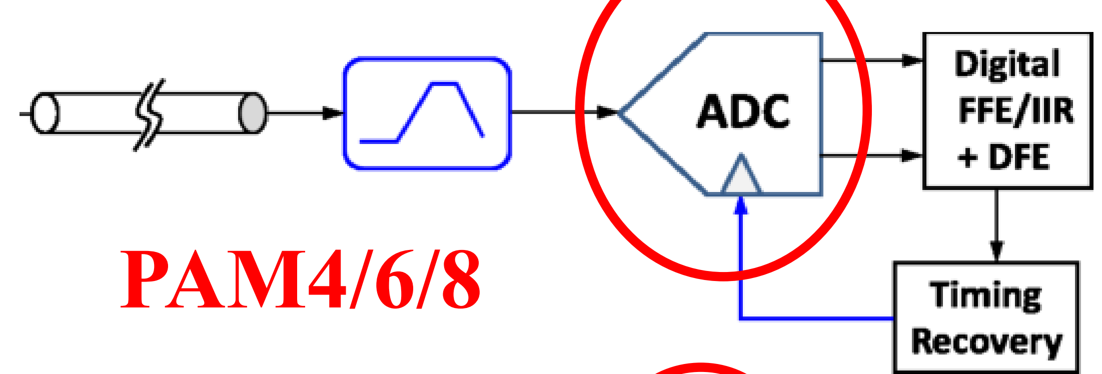
Per-lane data rate has doubled every 3-4 years.

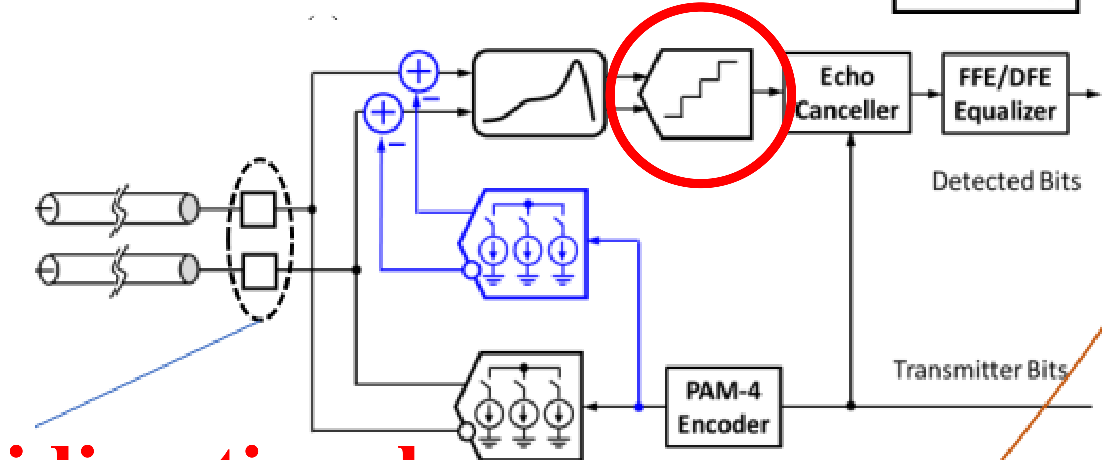
当前112Gb/s-SerDes-ADC+DSP已成为主流

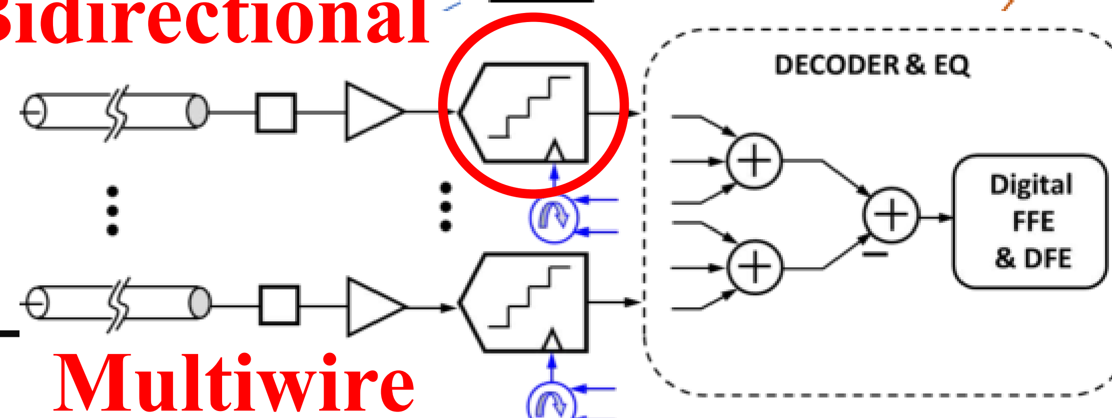
*	Process	DR (Gb/s)	TYPE	TX EQ	TX DRV	RX AEQ	RX STRUCTURE	POWER EFFE.	LOSS (dB)	REFERENCE
1	5nm	224 PAM-4	RX	-	-	CTLE/VGA	6BI TADC+DSP	1.41	31.6	Intel, ISSCC 2022
5	10nm	224 PAM-4	TX	8 FIR	DAC-CML	-	-	2.25	-	Intel, ISSCC 2021
2	5nm	112 PAM-4	TRX	6 FIR	DAC-SST	CTLE/VGA	7BIT ADC+30 FFE/1 DFE	4.5	40	Marvell, ISSCC 2022
3	7nm	60 PAM-4	TRX	7 FIR	DAC-SST	CTLE/VGA	14 DFE	3.03	47.5	Broadcom, ISSCC 2022
7	7nm	112 PAM-4	TRX	3-7 FIR	DAC-SST/CML	CTLE/VGA	7BIT ADC+25 FFE/2 DFE	5.9	45-52	Huawei, ISSCC 2021
8	7nm	112 PAM-4	TRX	4 FIR	DAC-CML	CTLE/VGA	ADC+DSP	6.51	>40	Inphi, ISSCC 2021
9	7nm	112 PAM-4	TRX	8 FIR	DAC-SST	CTLE/PGA	7 BIT ADC+32 FFE/1 DFE	8.2	26	eTopus Technology, ISSCC 2021
10	7nm	112 PAM-4	TRX	6 FIR	DAC-SST	CTLE/VGA	7BIT ADC+8-24 FFE/1 DFE	4.29	38.9	MediaTek, ISSCC 2020
11	7nm	112 PAM-4	TRX	4 FFE	CML	CTLE/PGA	7 BIT ADC+31 FFE/1 DFE	5.38	37.5	Xilinx, ISSCC 2020
12	7nm	10-112 PAM-4	TX	7 FIR	DAC-SST	-	-	1.56	-	Rambus, ISSCC 2020
13	14nm	100 PAM-4	RX	-	-	CTLE/VGA	8 FFE/1 DFE	1.1	20	IBM, ISSCC 2019
14	14nm	128 PAM-4	TX	3 FFE	CML	-	-	1.3	-	IBM, ISSCC 2019
15	40nm	112 PAM-4	TX	4 FFE	SST	-	-	3.89	5.5	Teletrx, ISSCC 2019
16	10nm	112 PAM-4	TX	3 FFE	CML	-	-	2.07	31	Intel, ISSCC 2018
17	14nm	112 PAM-4	TX	8 FFE	DAC-SST	-	-	2.6	-	IBM, ISSCC 2018
18	16nm	19-56 PAM-4	TRX	4 FIR	SST	CTLE/VGA	7 BIT ADC+14 FFE/1 DFE	9.7	32	Xilinx, ISSCC 2018
19	16nm	64 PAM-4	TRX	3 FFE	SST	CTLE/VGA	1+5BIT ADC+FFE/ DFE	5.84	29.5	University of Toronto, ISSCC 2018

下一代224Gb/s实现方案-ADC+DSP构架主导

		PAM-4 112 Gb/s	PAM-4 224 Gb/s	PAM-8 224 Gb/s	Multiwire Encoding 224 Gb/s	Bidirectional Signalling 224 Gb/s
Nyquist Frequency		28 GHz	56 GHz	39 GHz	67 GHz	28 GHz
channel	XSR-USR	$<10^{-6}$	$<10^{-6}$	$<10^{-3}$	$<10^{-8}$	$<10^{-5}$
	MCM	$<10^{-6}$	$<10^{-4}$	$>10^{-2}$	$<10^{-6}$	$<10^{-4}$
	Chip-to-module	$<10^{-6}$	$>10^{-2}$	$>10^{-2}$	$<10^{-4}$ (<45 dB) $>10^{-2}$ (>45 dB)	$<10^{-4}$
ADC Resolution		6 bit	6 bit	8 bit	5 bit	8 bit
ADC Power		1x	3x	2.8x	2.5x	3x
Equalizer		10 tap FFE & 1 tap DFE	10 tap FFE & 1 tap DFE	10 tap FFE & 1 tap DFE	8 tap FFE & 3 tap DFE	10 tap FFE & 1 tap DFE & 5-tap Echo-Canceller
Jitter Requirement		150 fs	80 fs	130 fs	125 fs	130 fs
Power		1x	2.8x	2.5 x	2.5 x	3x





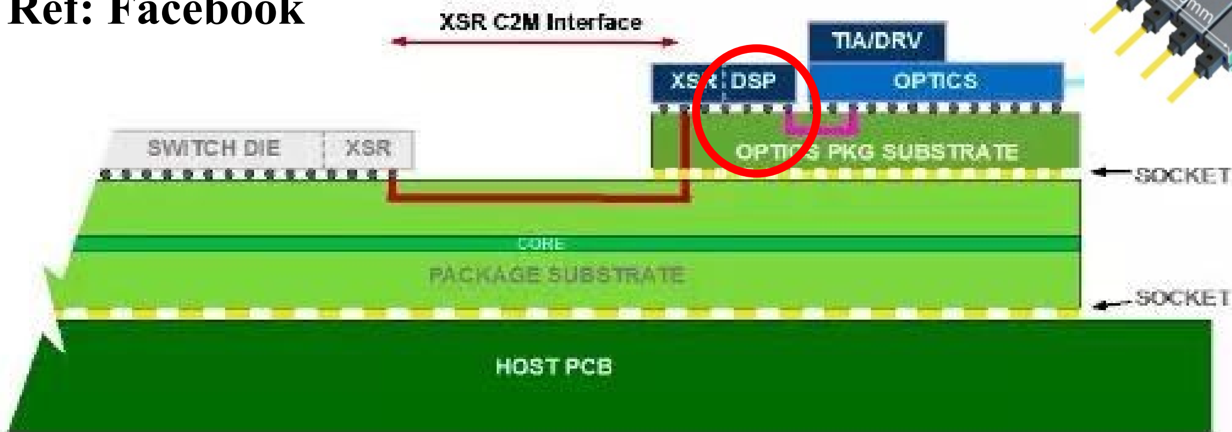


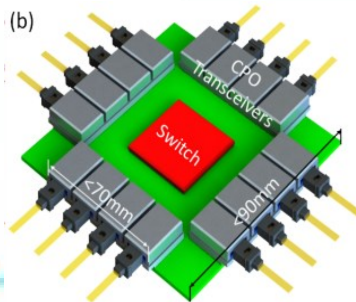
下一代224Gb/s的备选实现方案均基于ADC+DSP构架

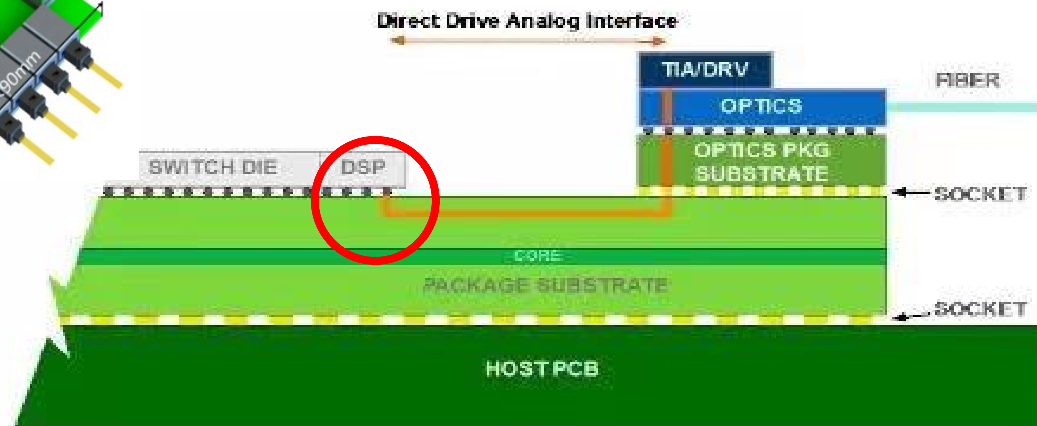
Ref：2021-TCPM-Toward 224-Gb/s Electrical Signaling—Modulation, Equalization, and Channel Options

CPO-DSP依然不可或缺

Ref: Facebook







- **Switch Generation:** 51.2T
- **Lane Speed:** 106 Gb/s
- **Interface Architecture:** XSR based AUI, 400G-FR4 PMD (& 200G-FR4 down-speed)
- **Motivation:** System Power Reduction, Ecosystem & Operational Readiness

- **Switch Generation:** 102.4T
- **Lane Speed:** 212 Gb/s (?)
- **Interface Architecture:** Direct-Drive to Optics (analog) 800GBASE-FR4 compatible (& 400G-FR4)

[Requires new standardization work on direct drive. note: will not support BiDi, or lane gearboxing]

- **Motivation:** System Power Reduction & Bandwidth Scaling (Densification)

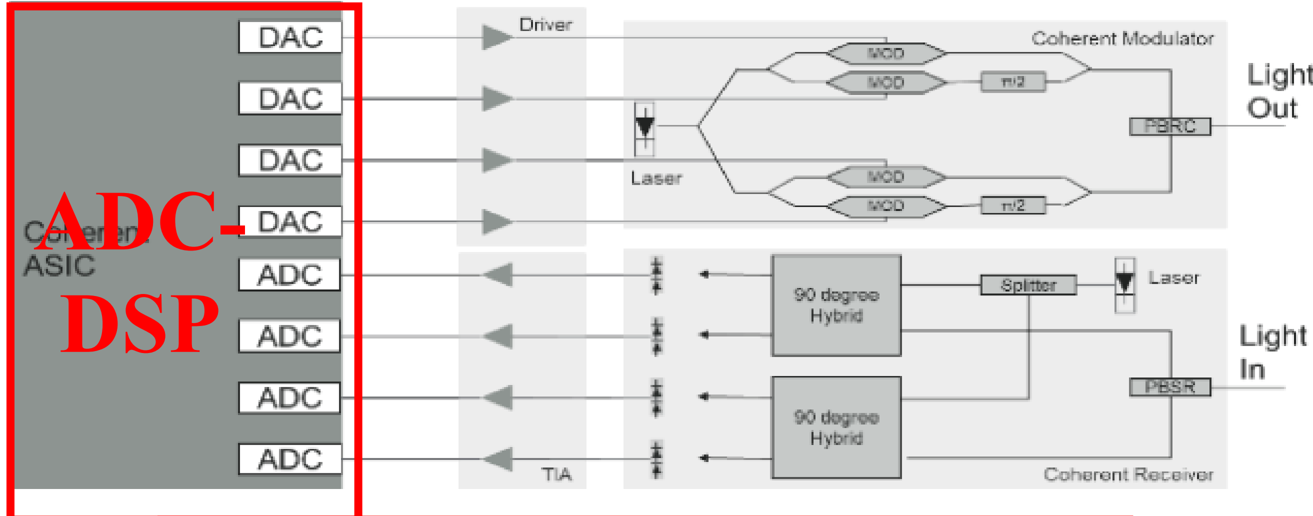
Facebook – OIF CPO Webinar 2020

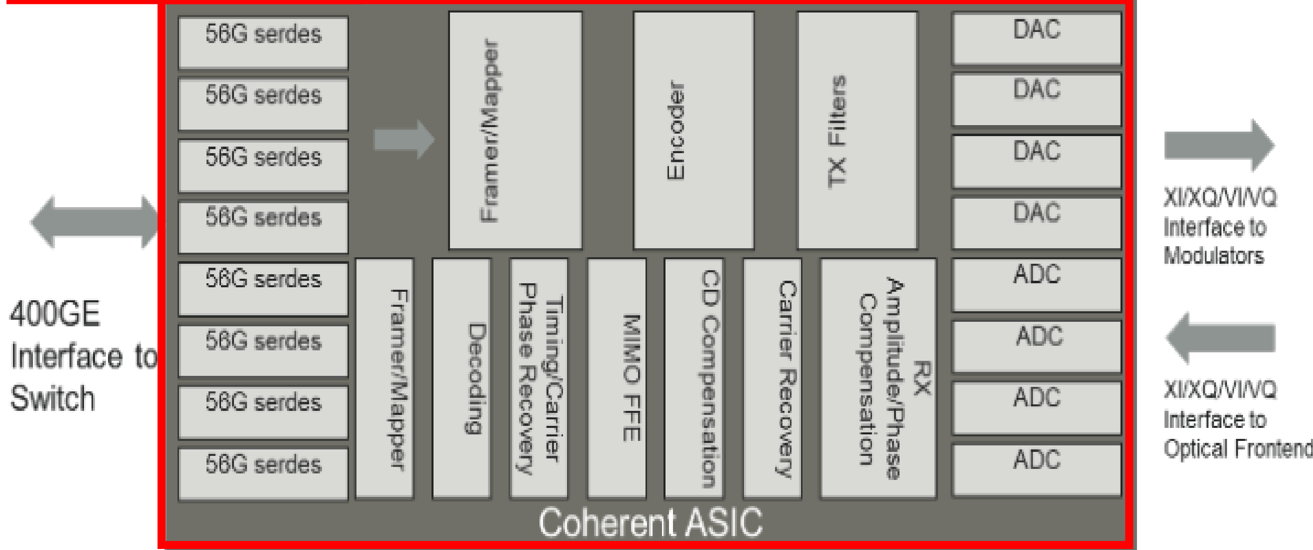
Target: Lower Power

Method: Short Connection Distance

DSP: Optical Loss, dispersion, nonlinearity…

400G-ZR 相干光通信-ADC+DSP核心芯片





Ref: OFC-2022-Marvell-Development of Low-power Coherent ASIC

Table 1: Definition of an ASIC for 400ZR

Type of line interface	400ZR
Symbol rate of line interface	59.87GHz
Number of electrical lanes	4
Modulation of line interface	DP-QAM16
FEC of line interface	C-FEC with 15% overhead
Pilot overhead of line interface	3%
ROSNR Tolerance	26db
Chromatic Dispersion Tolerance	2400ps/nm
Type of Host interface	400GAUI-8
Number of host lanes	8
Symbol rate of host interface	26.5625GHz
Modulation of host interface	PAM4
FEC of host interface	RS(544,514)
Link Loss Budget	10.2db

Bandwidth: 40GHz

Sample rates：97Gsamples/s

Resolution：8bit

Jitter：150fsrms

Energy Efficiency：35fJ/conversion-step

ASIC Energy Efficiency: 40-60pJ/bit

2.5D/3D 短距相干光通信-ADC+DSP变化不大

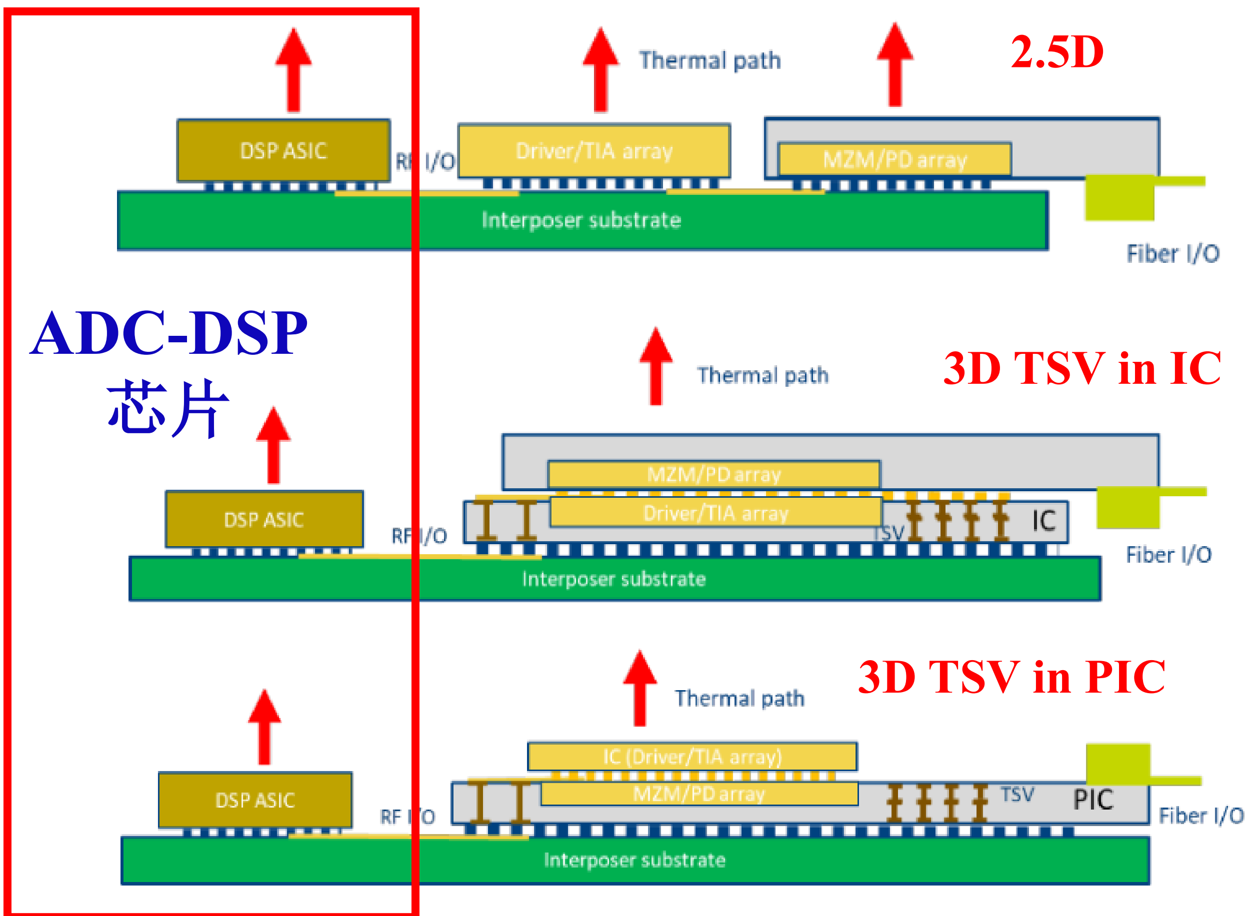


Fig. 5. 2.5D/3D silicon photonic-electronic integration with PIC, IC and DSP, and optical I/O and RF I/O for coherent transceiver without TSV in IC and PIC as 2.5D (upper), TSV in IC as 3D (middle), and TSV in PIC (lower).

Table 8 Power budget for 6.4T/s coherent transceiver

	Power, W	Efficiency, pJ/bit
Integrated IC/PIC		
PIC	**2.5**	**0.4**
Driver	**16.3**	**2.6**
TIA	**12.8**	**2.0**
Integrated IC/PIC	**31.6**	**4.9**
DFB lasers		
4 LO Lasers	**4.4**	**0.7**
4 Tx lasers	**5.8**	**0.9**
Total 8x DFB Lasers	**10.3**	**1.6**
Transceiver optics (IC/PIC + lasers)		
Transceiver optics	**41.9**	**6.5**
DSP ASIC predicted		
DSP ASIC, predicted	**32.0**	**5.0**
Transceiver		
Misc, predicted	**2.0**	**0.3**
Transceiver, predicted	**75.9**	**11.9**

提 纲

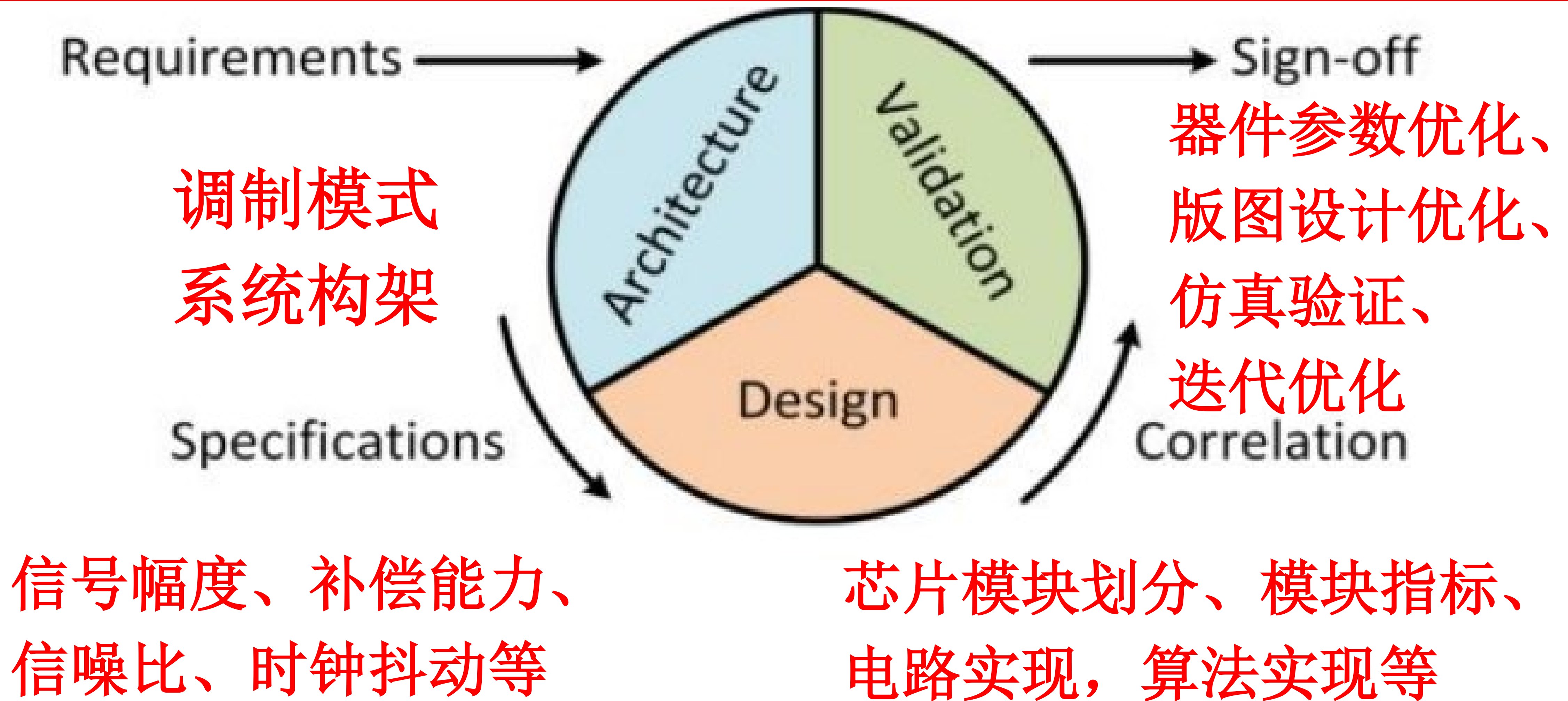
- SerDes发展趋势与应用场景
- SerDes研究方法与关键技术
  - 系统级建模与仿真
  - 电路级技术演进
- 基于ADC/DSP PAM4 收发机

高速串行接口通信核心问题

高速串行接口演进驱动力：用尽量低的功耗、面积及链路成本解决好尽量高速率下的横向时序和纵向信噪比的信号完整性问题。

- 纵向信噪比：数据均衡设计---**Data Path**
- 横向时序：　时钟定时设计---**Clock Path**
- 高速率：　　宽带扩展设计

高速SerDes的设计阶段



调制模式
系统构架

器件参数优化、
版图设计优化、
仿真验证、
迭代优化

信号幅度、补偿能力、
信噪比、时钟抖动等

芯片模块划分、模块指标、
电路实现，算法实现等

Ref: 2022-DesignCon-Aleksey Tyshchenko, et. al-Parametric System Model of a 112Gbps ADC-based SerDes for Architectural, Design & Validation Project Phases

System-Level-Simulation-统计仿真（COM）

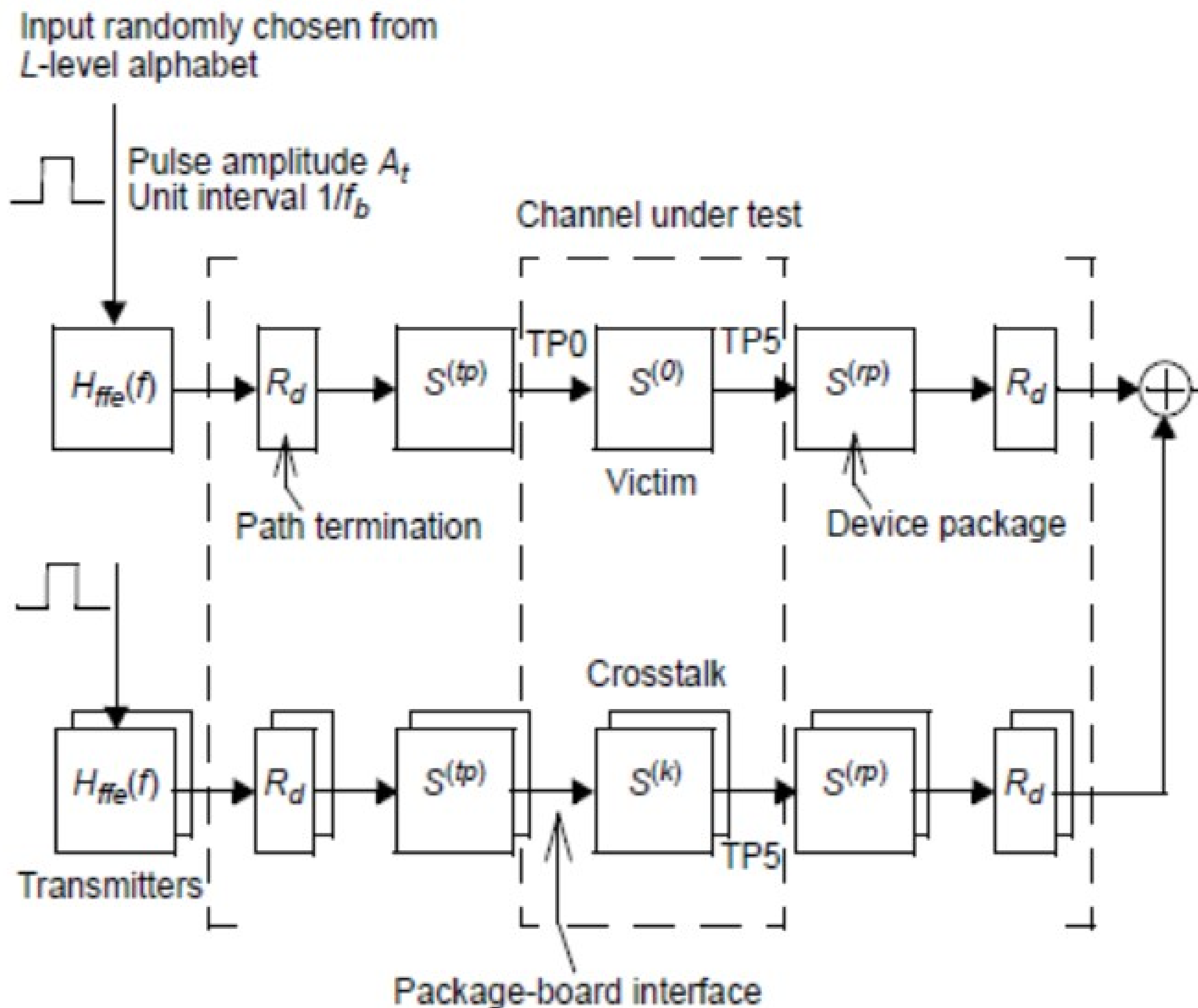
基于SerDes电气约束验证实际信道对通信标准的满足情况

特点

- LTI线性时不变系统
- 纵向幅度统计特性分析

挑战

- 非线性问题
- 横向抖动特性分析
- 精度问题



COM Reference Model

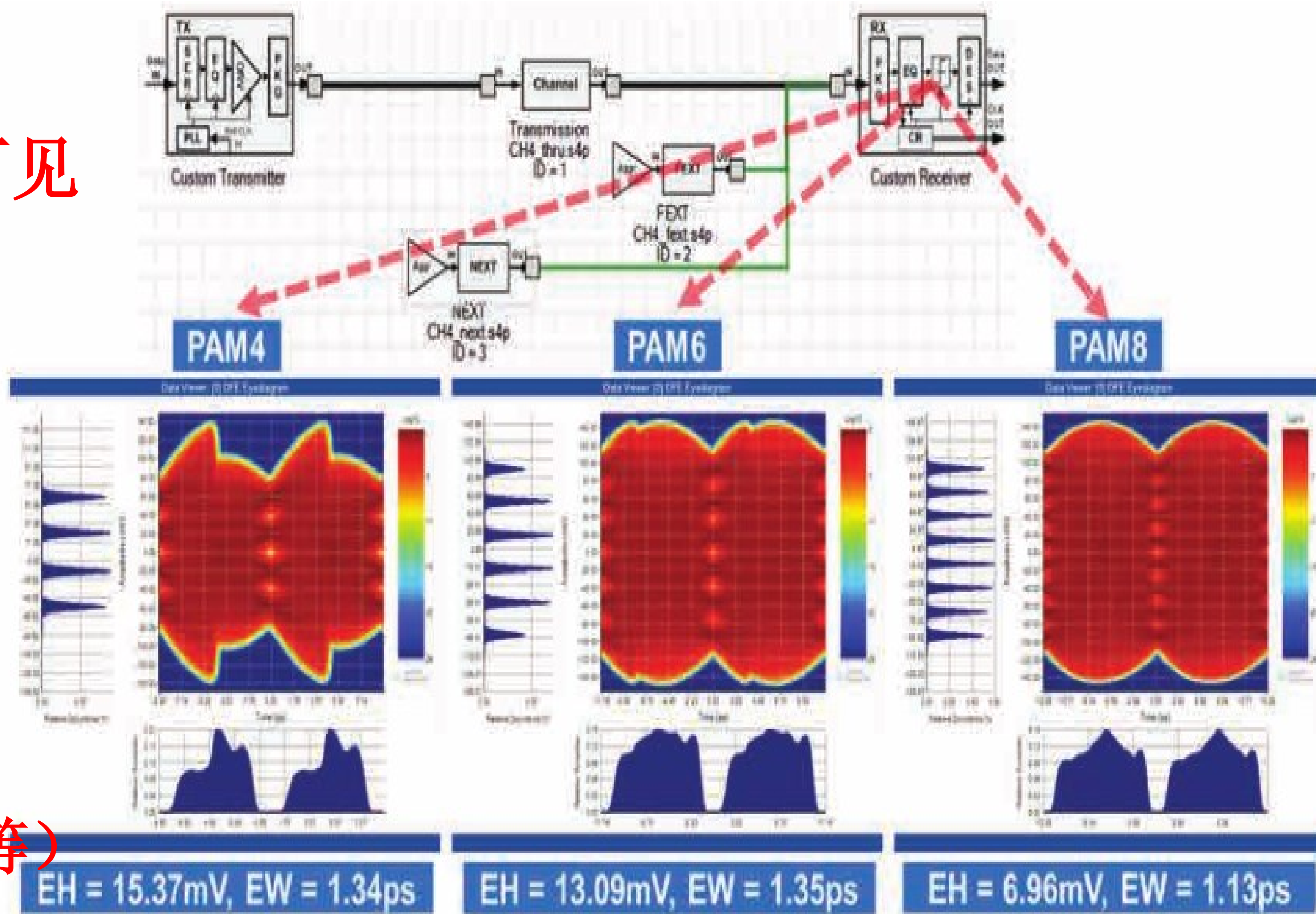
System-Level-Simulation-时域bit-by-bit链路仿真

优势

- 时域模型-波形直观可见
- 模型可分析纵向噪声
- 模型可分析横向抖动

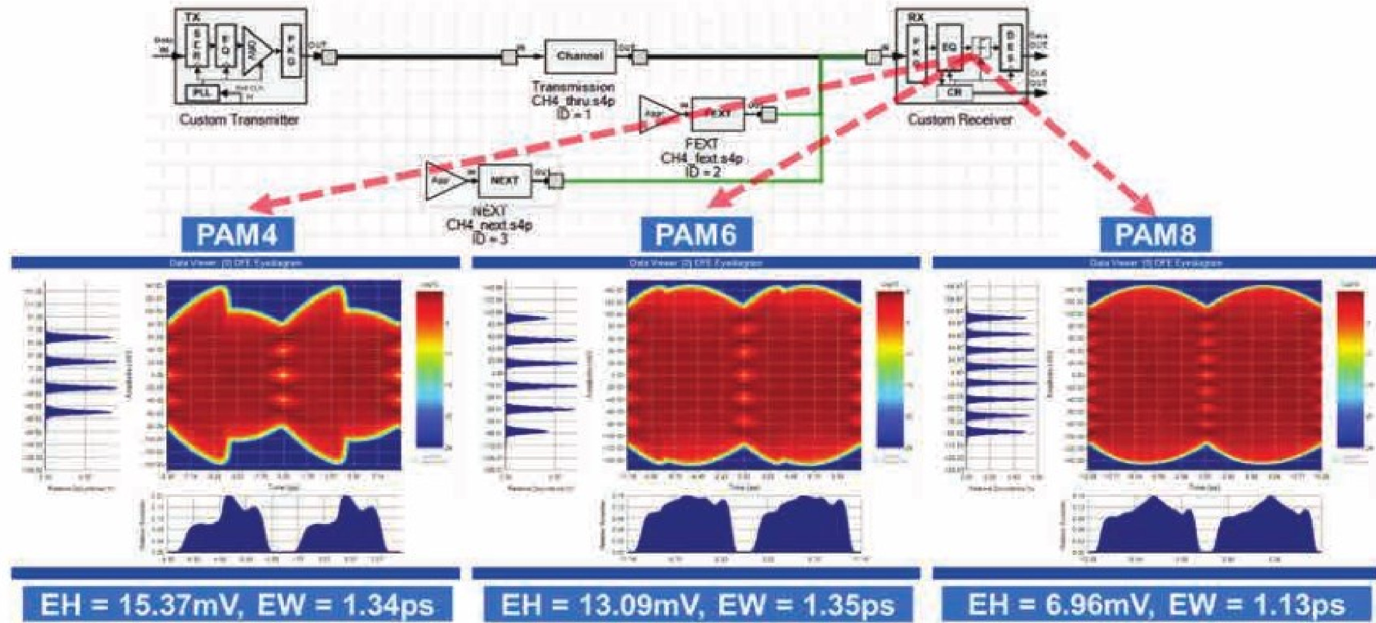
挑战-精度问题

- 噪声精度
- 抖动精度
- 模拟电路特性
- 工作环境（PVT，供电等）



Ref 2022-SI-224 Gb/s Modulation and Channel Characteristics

System-Level-Simulation-时域bit-by-bit链路仿真



Ref 2022-SI-224 Gb/s Modulation and Channel Characteristics

研究积累与设计基础

Simulation Configuration:

- Data Rate: 224 Gb/s
- Modulation Scheme: PAM4, PAM6, PAM8
- Test Pattern: PRBS-31 with PAM4/PAM6/PAM8 coding

Transmitter Configuration:

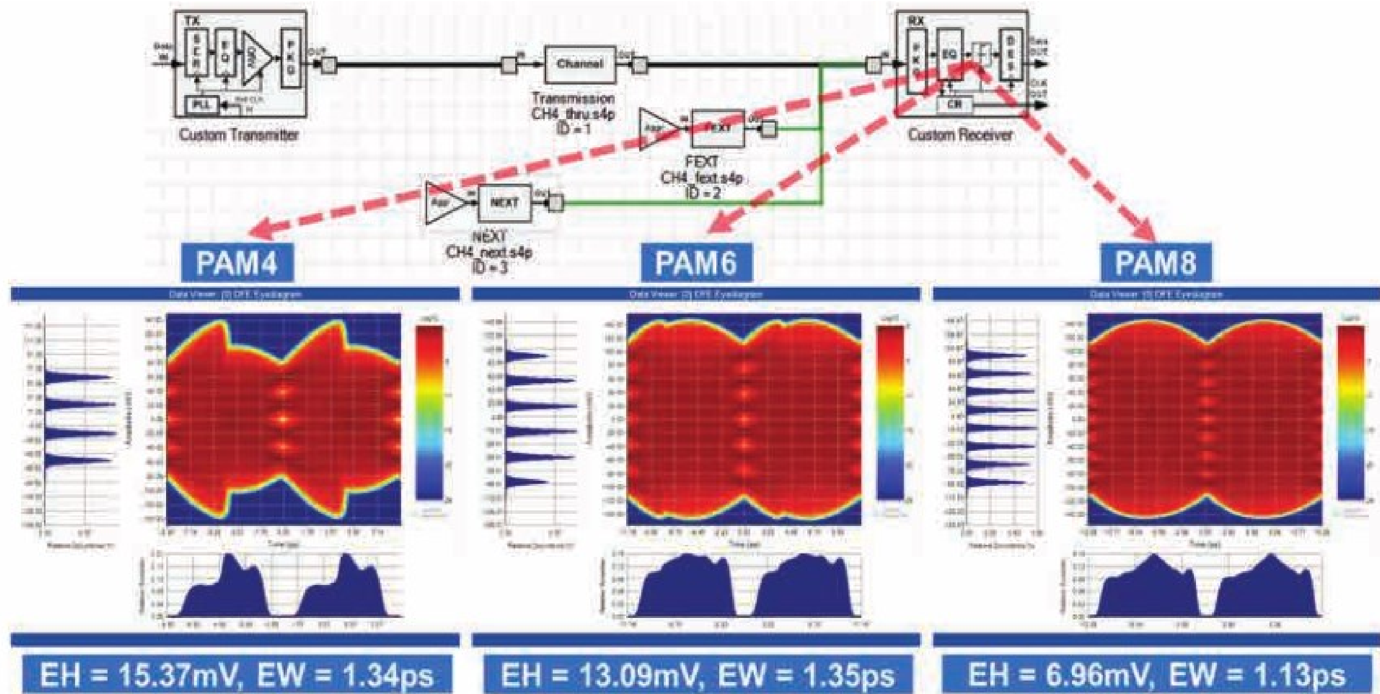
- 20 to 80 percent Rise/Fall Time: Correlated to Intel 224 Gb/s test chip[1]
- AFE Characteristics: Correlated to Intel 224 Gbps test chip[1]
- TX EQ: 4 pre-taps and 1 post-tap
- Separation Level Mismatch (RLM): 0.95
- Jitter: duty-cycle distortion (DCD): 0.019 UIpeak-peak, bounded uncorrelated jitter (BUJ): 0.04 UIpeak-peak, random jitter (RJ): 0.01 UIRMS
- Noise: 11.19 mVRMS (corresponding to transmitter output SNR of 33 dB)
- Package: 31 mm, per Intel package 2024-2025 projection

Receiver Configuration:

- AFE Characteristics: Correlated to Intel 224 Gbps test chip[1]
- RX EQ: continuous time linear equalization and RX FFE+DFE: three pre-tap, 24 post-tap, floating taps with six banks of three consecutive taps up to 80 taps
- RX Jitter/Noise: RX input referred noise: 4.1x10-9 V2/GHz
- Package: 29 mm, per Intel package 2024-2025 projection. The channel characteristics of all test channels is shown in

- 研究积累：系统构架/均衡方案/抖动分配等
- 原型芯片测试数据：转换沿/关键模块特性
- 封装测试数据；信道衰减串扰；
- 原理性分析：输出噪声/输入参考噪声；
- 编程与分析能力等

System-Level-Simulation-时域bit-by-bit链路仿真



① 新调制模式探索与传输信道需求

- 不同调制模式比较
- 不同信道的效果比较

Ref 2022-SI-224 Gb/s Modulation and Channel Characteristics

② 系统级指标分频

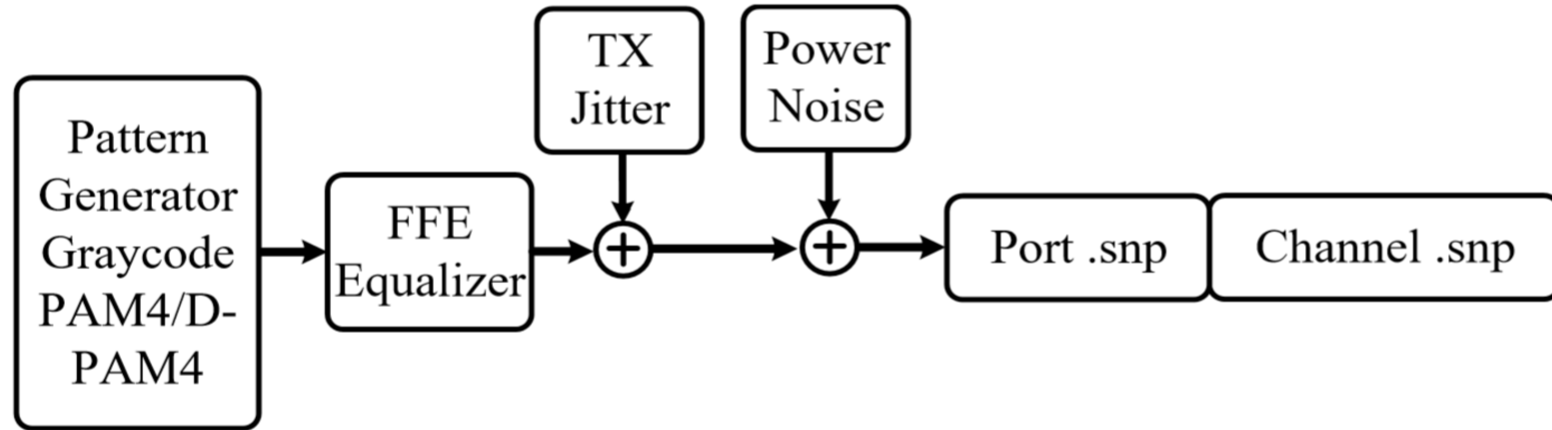
- 信号幅度、
- 补偿能力、
- 信噪比、
- 时钟抖动等

③ DSP算法验证

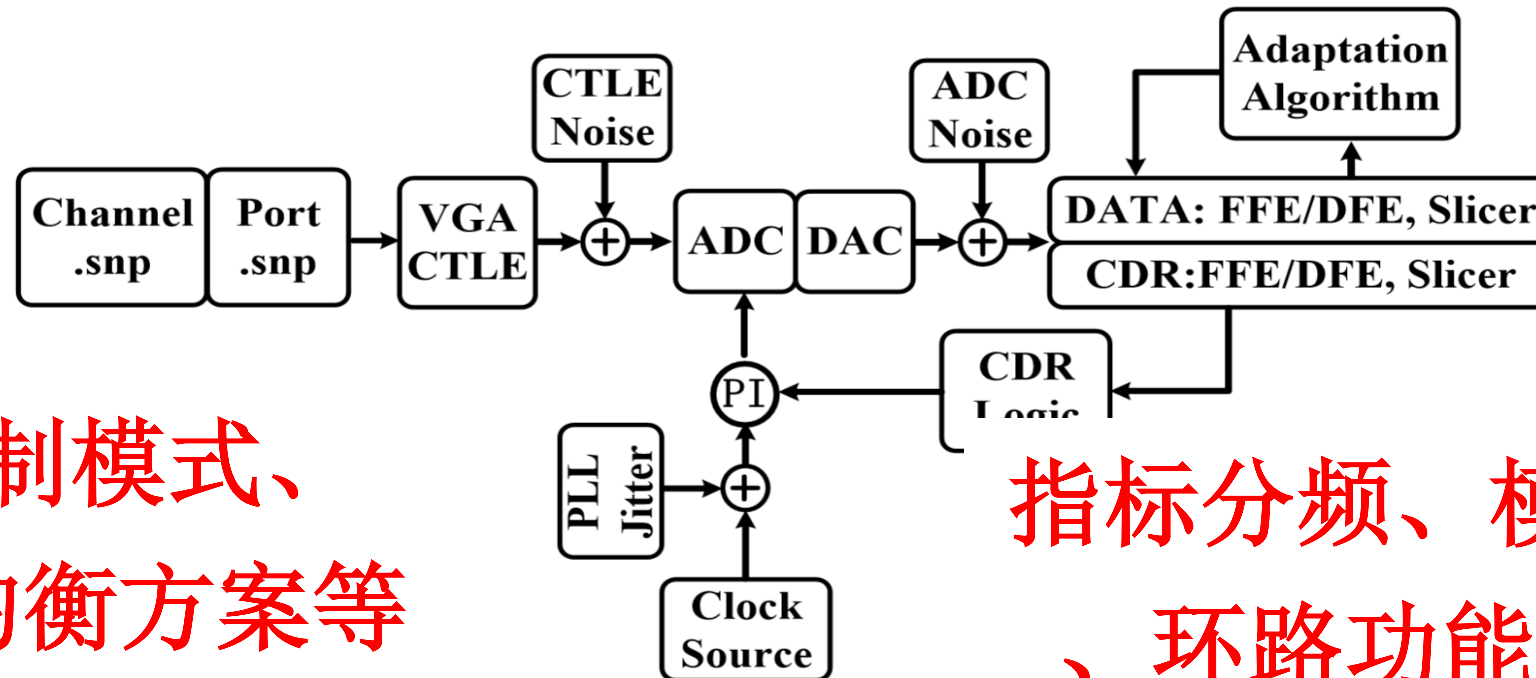
- ADC校准算法
- FFE/DFE实现
- CDR设计实现
- 自适应算法

System-Level-Simulation-时域bit-by-bit链路仿真

发送端模型



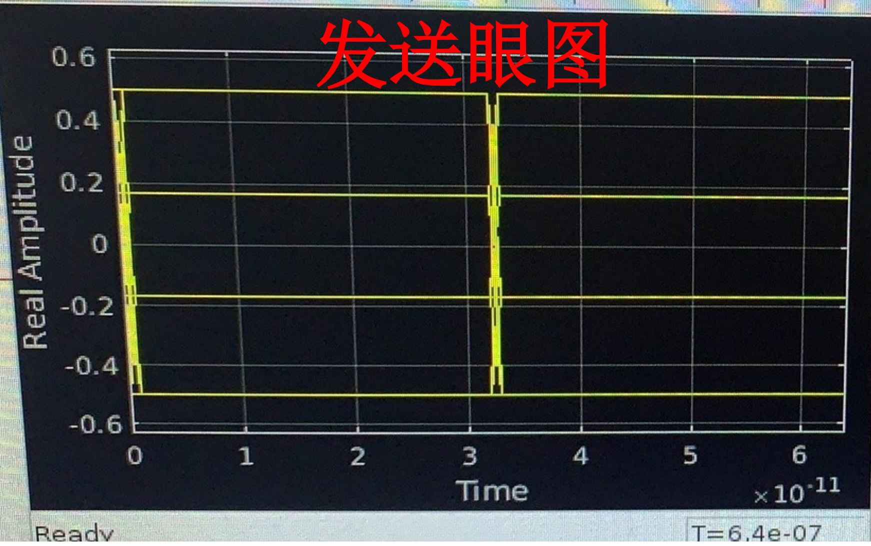
接收端模型

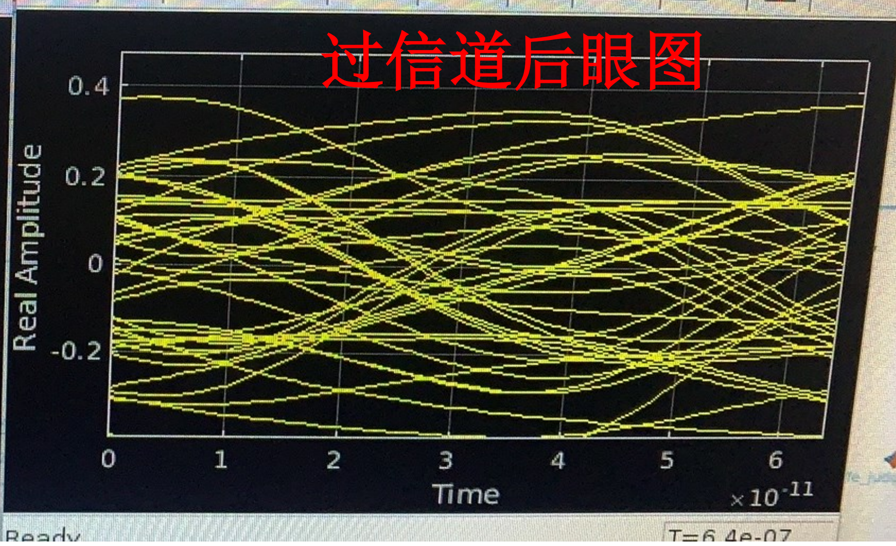


探索新的调制模式、系统构架、均衡方案等

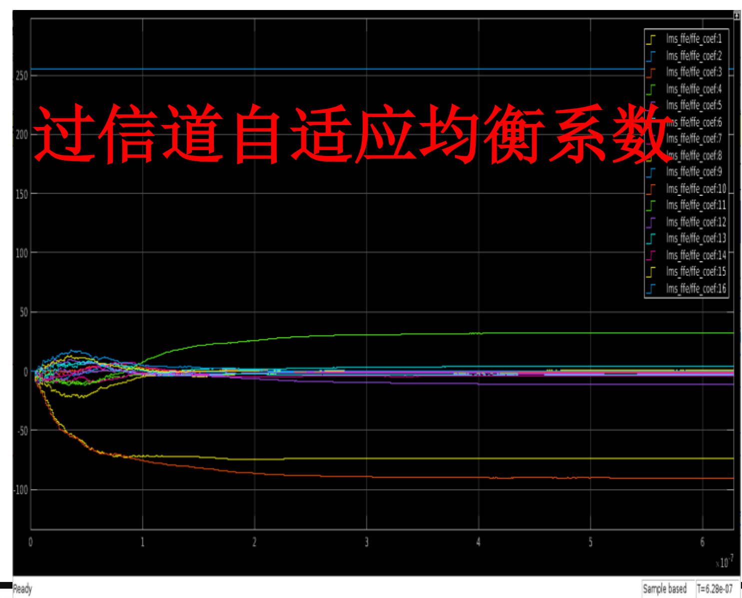
指标分频、模块开发、环路功能验证等

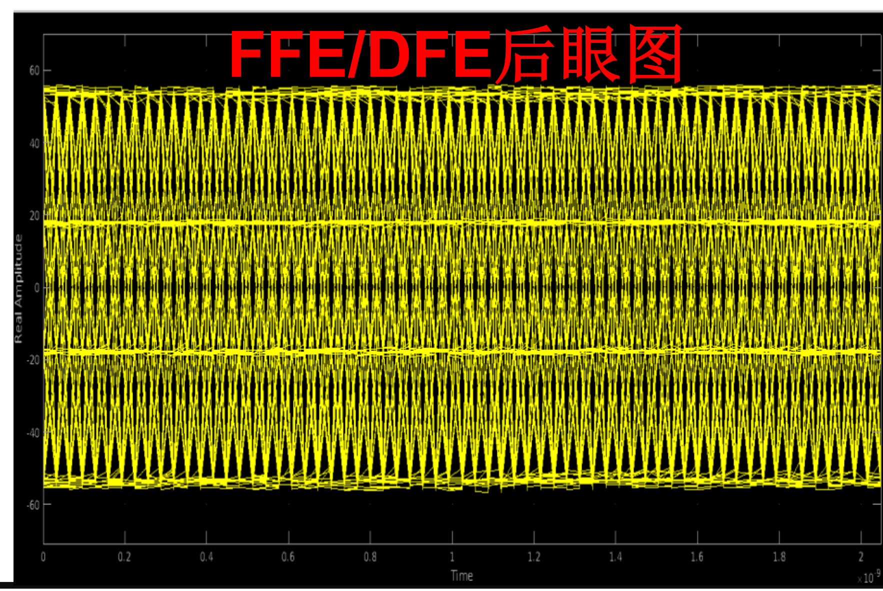
System-Level-Simulation-时域bit-by-bit链路仿真

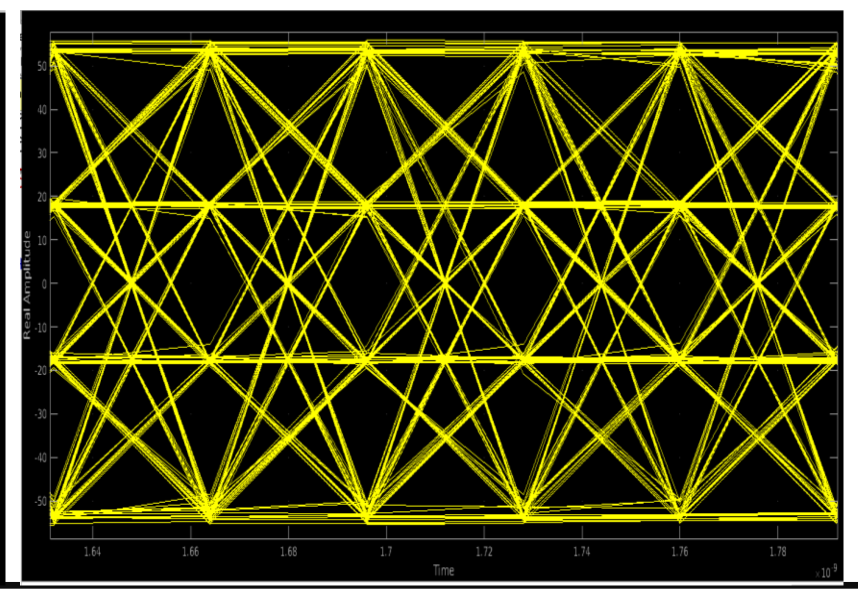




环路自适应
算法级验证





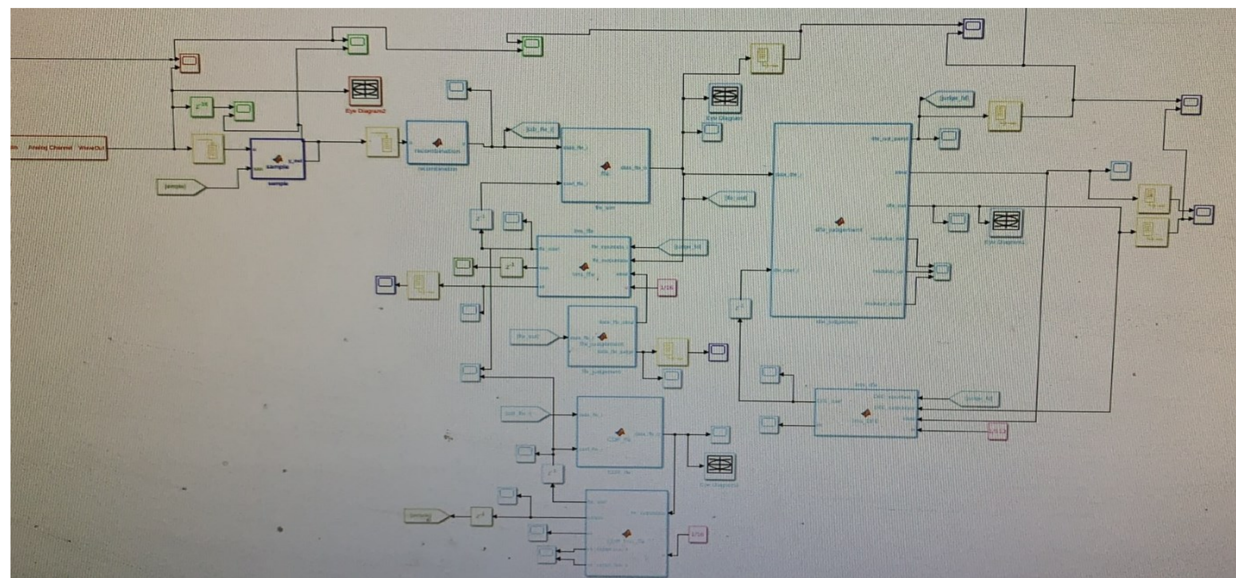


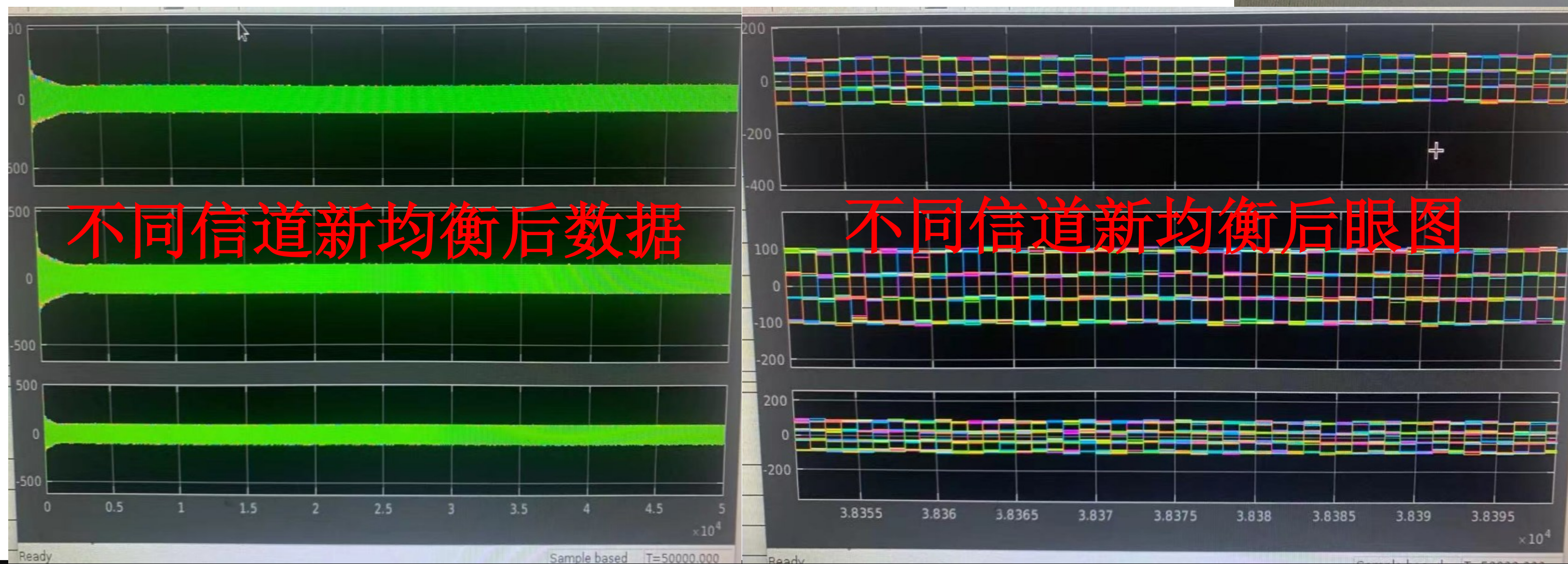
Matlab+RTL-时域bit-by-bit链路仿真

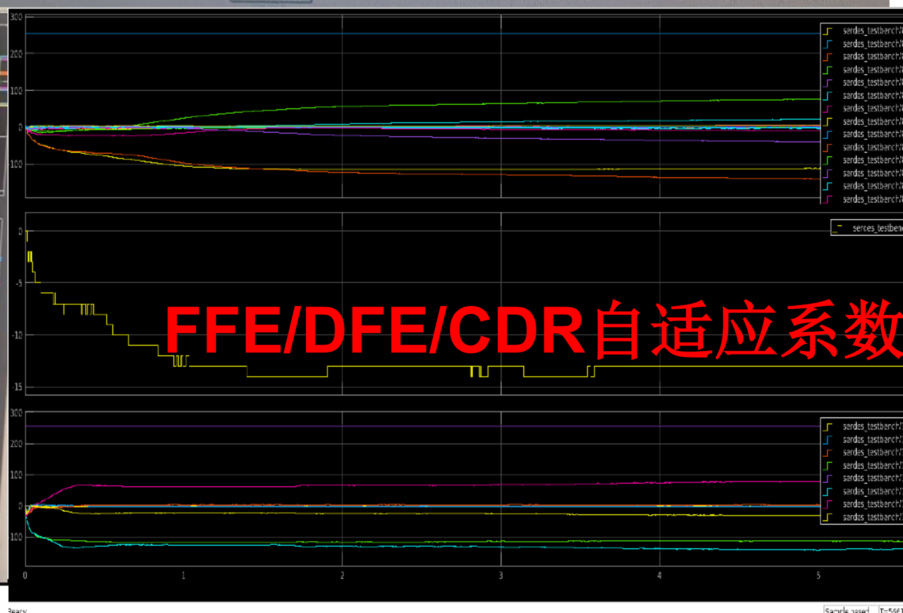
实现自适应环路的RTL级验证

DSP中RTL代替Matlab

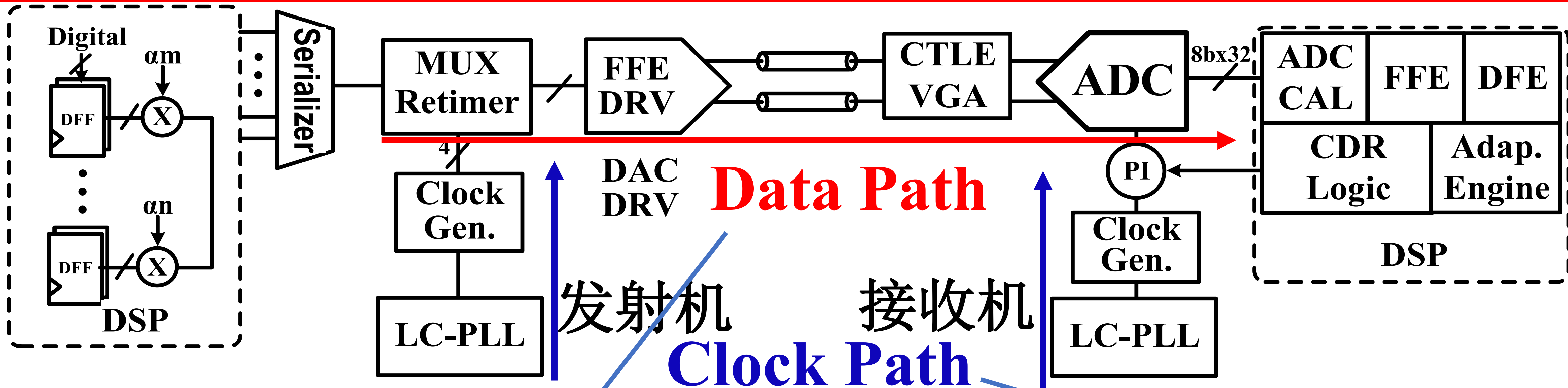
- 引入实际时序
- 有限位精度取代浮点型精度







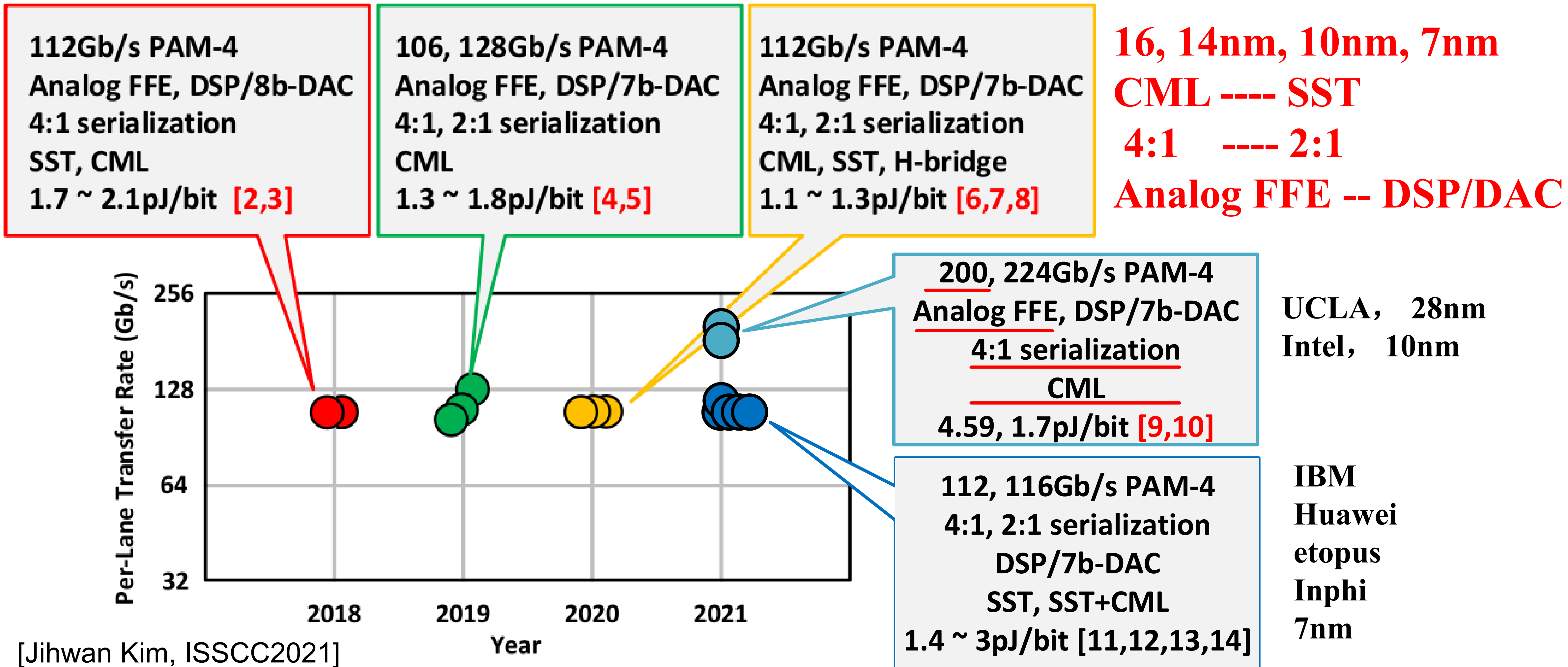
ADC/DSP-Based LR SerDes -主要技术特征



- Precise Timing
- High Bandwidth
- Large Swing
- High Linearity
- Adaptive Equalization

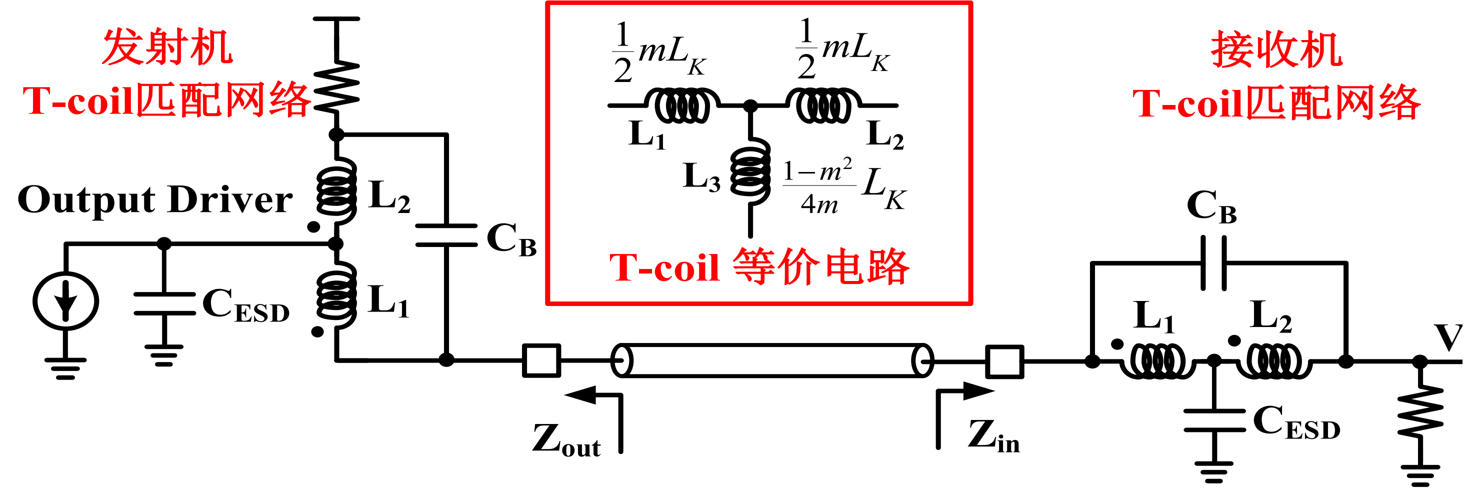
- Low Jitter
- Precise Phase
- Strong Tracking Ability

LR SerDes 发射机进展

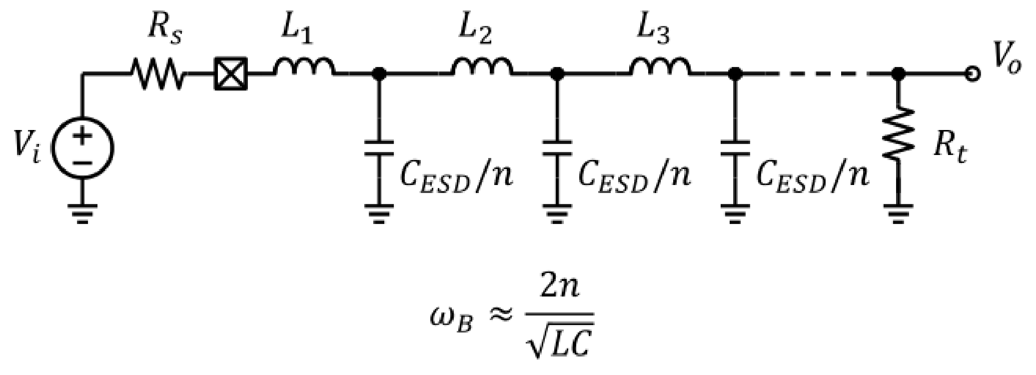


Published in ISSCC in last four years

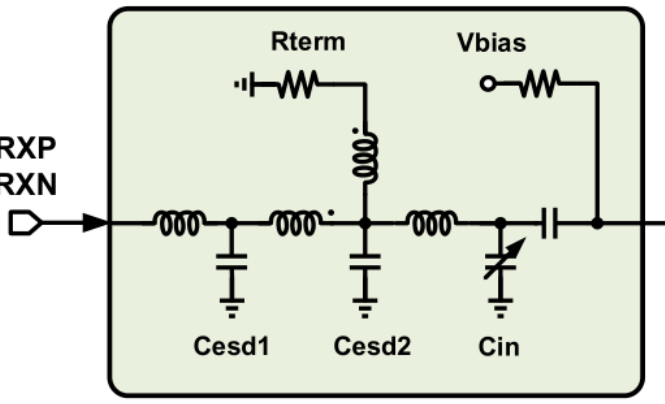
数据通路-接收机-宽带匹配



eTopus 56/112G, ISSCC2022



Alphawave 200G PAM4, ISSCC2022

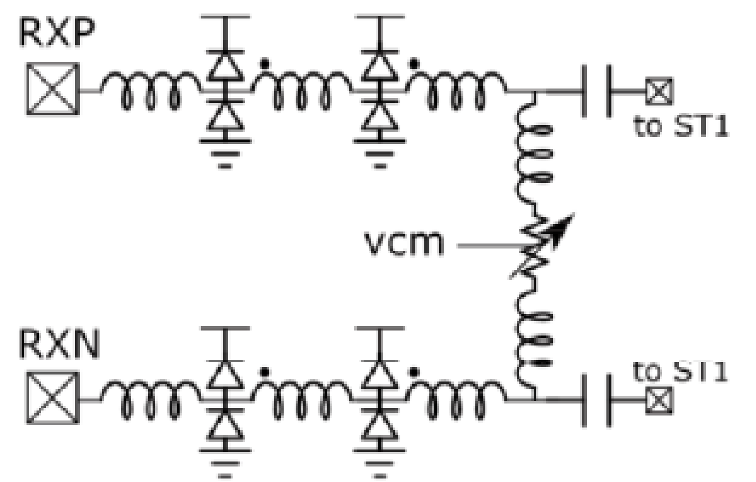


Marvell 112G, ISSCC2022
Inphi 112G, ISSCC2021

56/112G
Tcoil/Tcoil Variants

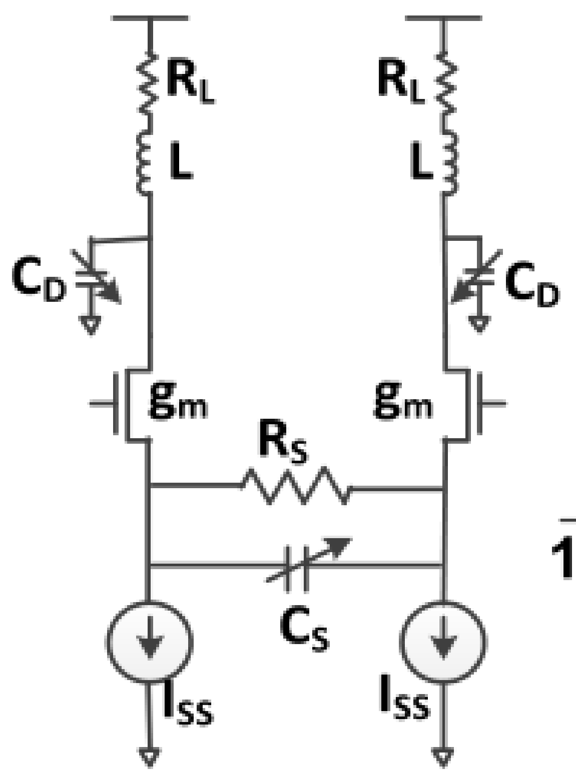
>200G
Artificial Transmission Line

Higher Speed



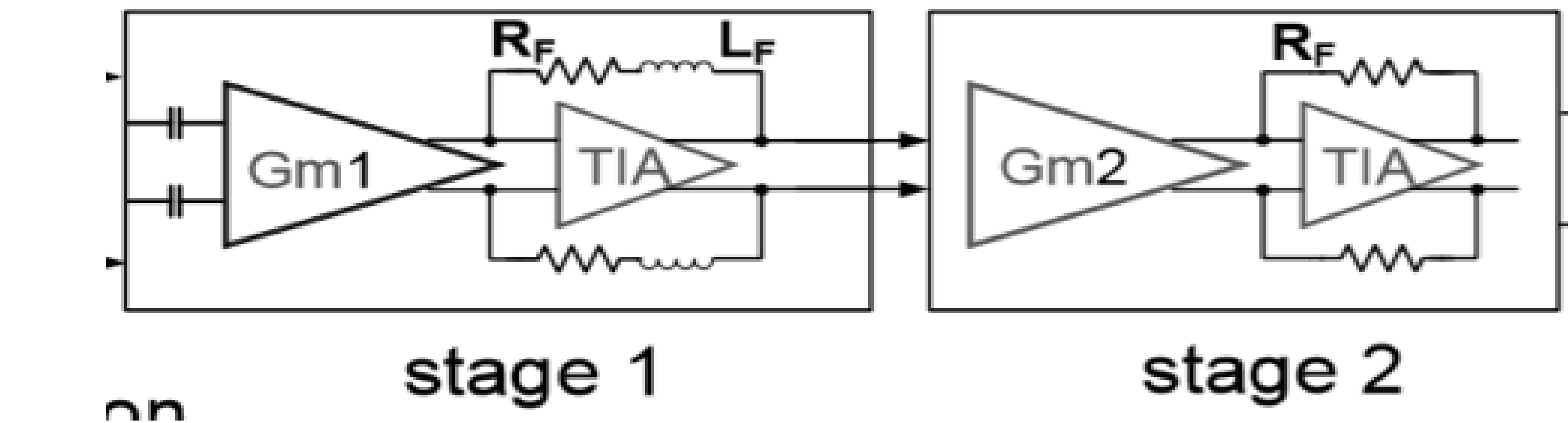
Intel 200G PAM4, ISSCC2022

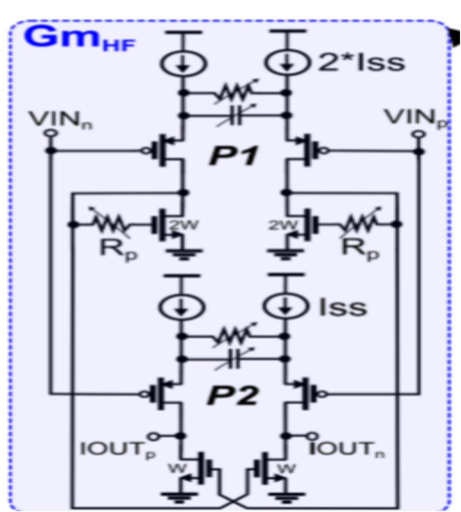
数据通路-接收机-CTLE

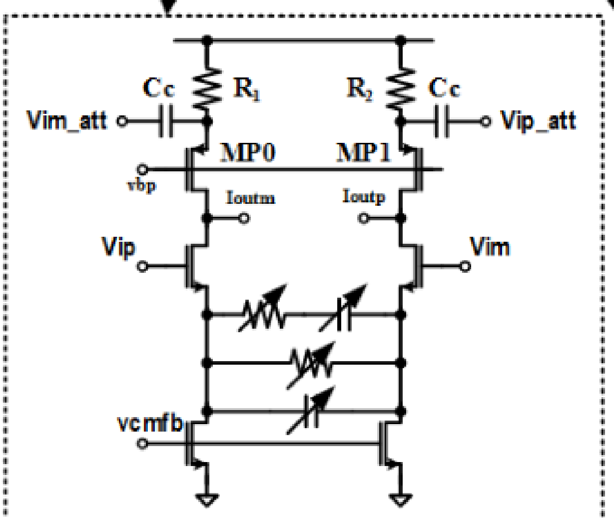


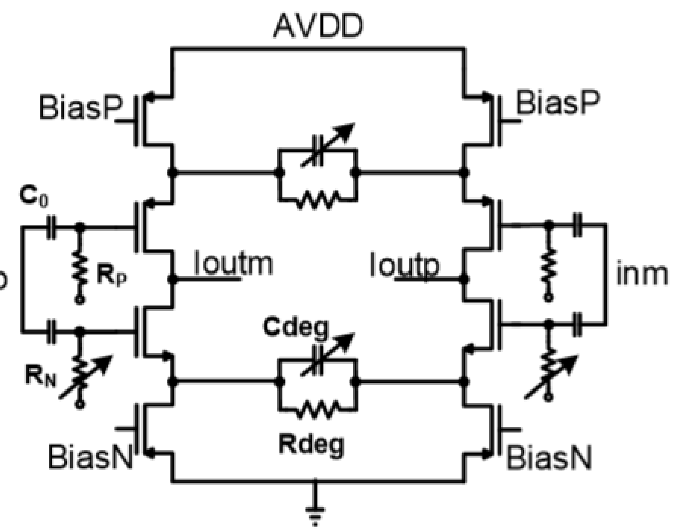
Inductive peaking
Source degeneration

Xilinx 56G , JSSC2017
Inphi 112G,ISSCC2021





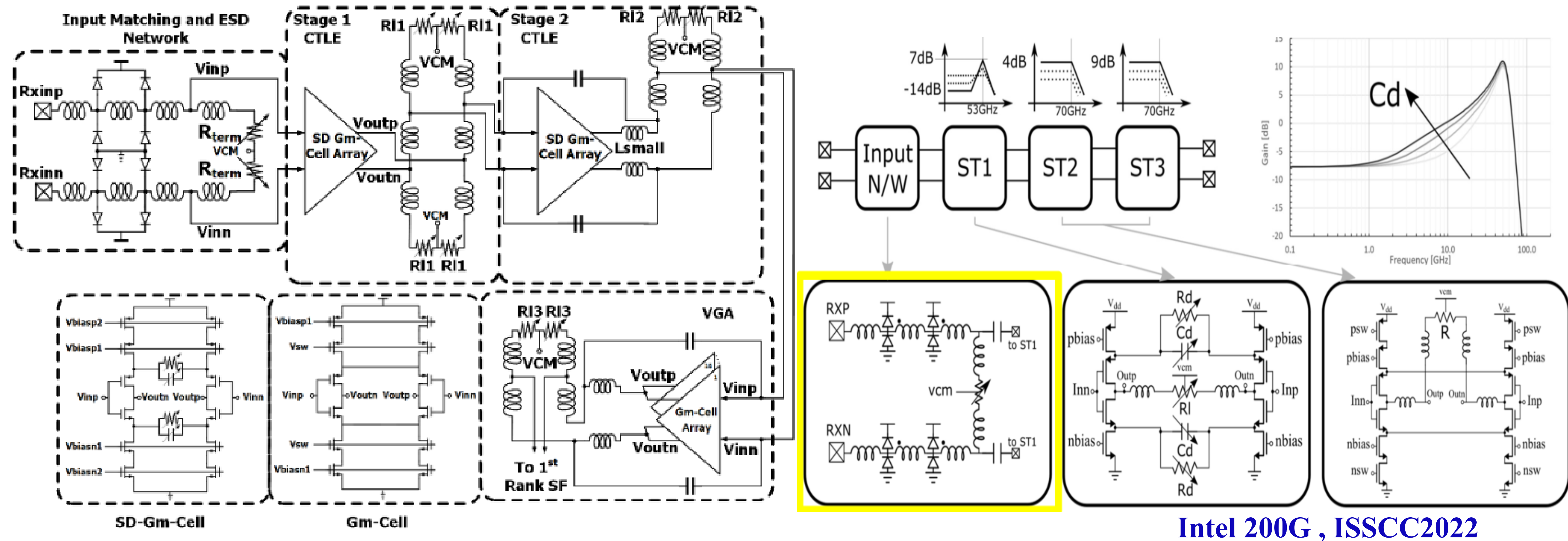




Gm-TIA Topology to Archive High Bandwdith

IBM 112G , ISSCC2019　Huawei 112G , ISSCC2021　Marvel 112G , ISSCC2022

数据通路-接收机-CTLE

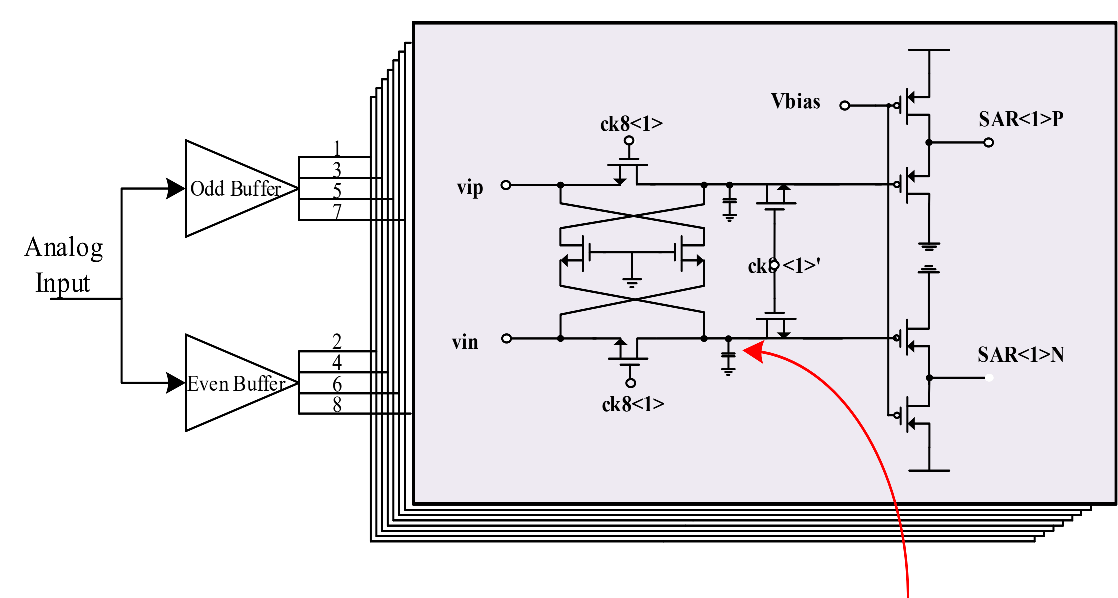


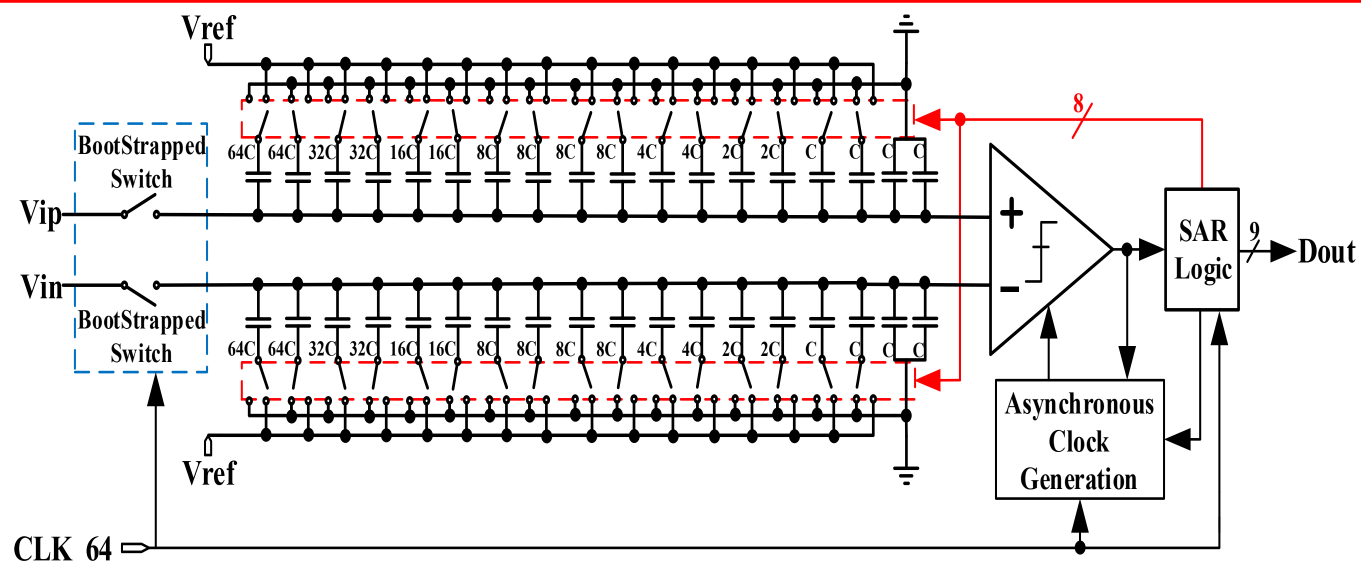
Intel 200G , VLSI2021

Negative Miller C extend bandwidth (S1)
Small Ls extend bandwidth (S2)

CMOS driving architecture
Inductive peaking and source degeneration (CTLE)
Series-shunt inductive peaking (VGA)

数据通路-接收机-ADC



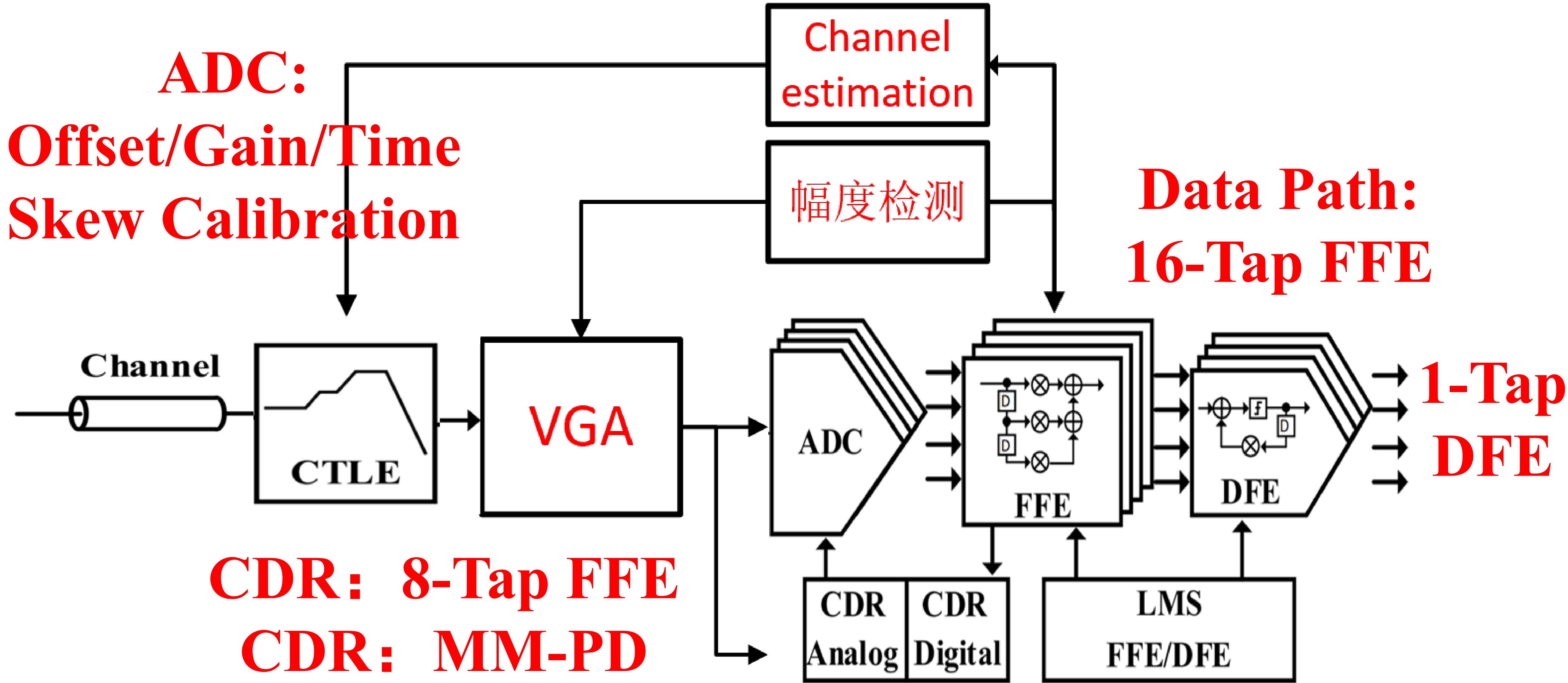


- 8X8 模拟前端，带宽超过25GHz，交织前端功耗100mW
- 顶板采样技术，Splitting & Monotonic的开关策略
- 采用Double-Tail比较器，动态失调校准电路
- 6-8bits模式调节

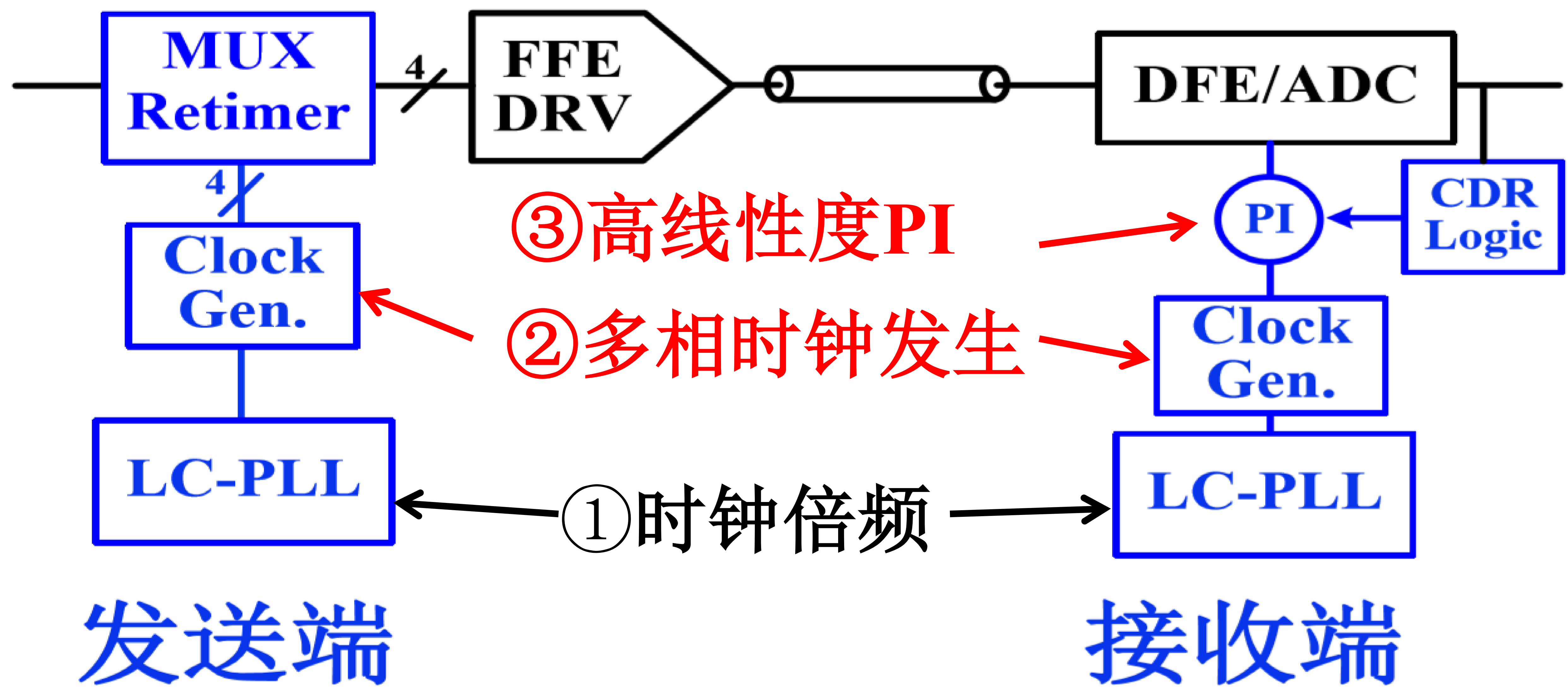
小面积
小寄生
小功耗

速度：1GS/s；功耗：3.5mW；摆幅：500mV；SFDR:>55dB；ENOB:>6.5

数据通路-接收机-DSP



时钟通路



时钟通路-基于DLL的多相时钟产生

主要优势

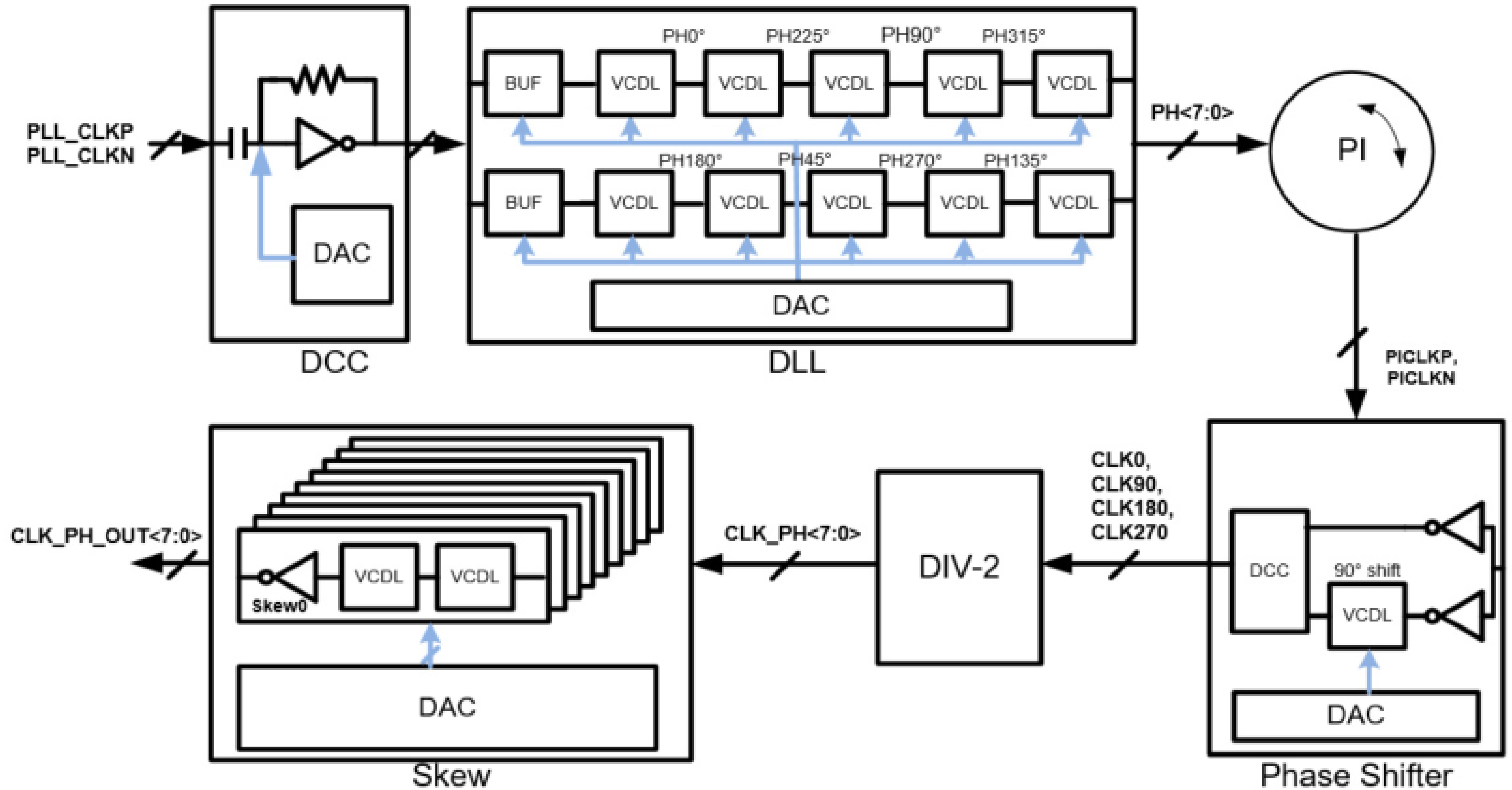
环路稳定

主要挑战

DLL校准

X2校准

功耗



Marvel ISSCC2022

时钟通路-基于ILO的多相时钟产生

主要优势
紧凑简洁
低功耗

三个挑战
频率追踪
锁定范围
相位拉拽

Xilinx ISSCC2020

提 纲

- SerDes发展趋势与应用场景
- SerDes研究方法与关键技术
  - 系统级建模与仿真
  - 电路级技术演进
- 基于ADC/DSP PAM4 收发机

基于ADC-DSP 高速SerDes设计体会

① **系统复杂、涉及模块多**: 基准、偏置、LDO、ADC、DAC、 PLL、 CDR、FFE/DFE、Adaptation Algrithom、 Calibration

② **知识密集、涉及学科多**：模集、数集、射频、微波、信号与系统、数字信号处理、matlab、systemverilog、EMX/HFSS

③ **协同要求高、涉及工种多**：系统建模工程师、模拟电路工程师、射频微波工程师、模拟版图工程师、数字前端工程师、数字验证工程师、数字后端工程师、封装设计工程师、PCB设计工程师、测试工程师

④ **工艺要求高**: 产品团队的不能做，培养团队的做不起。

Year of Production	2012	2015	2017	2019	2022	2025
CMOS node	40nm	28nm	16nm	7nm	3nm	2.1nm
Power, W/100G	50	20	7	2	1	0.5
Power efficiency, pJ/bit	500	200	70	20	10	5

谢谢！

欢迎交流